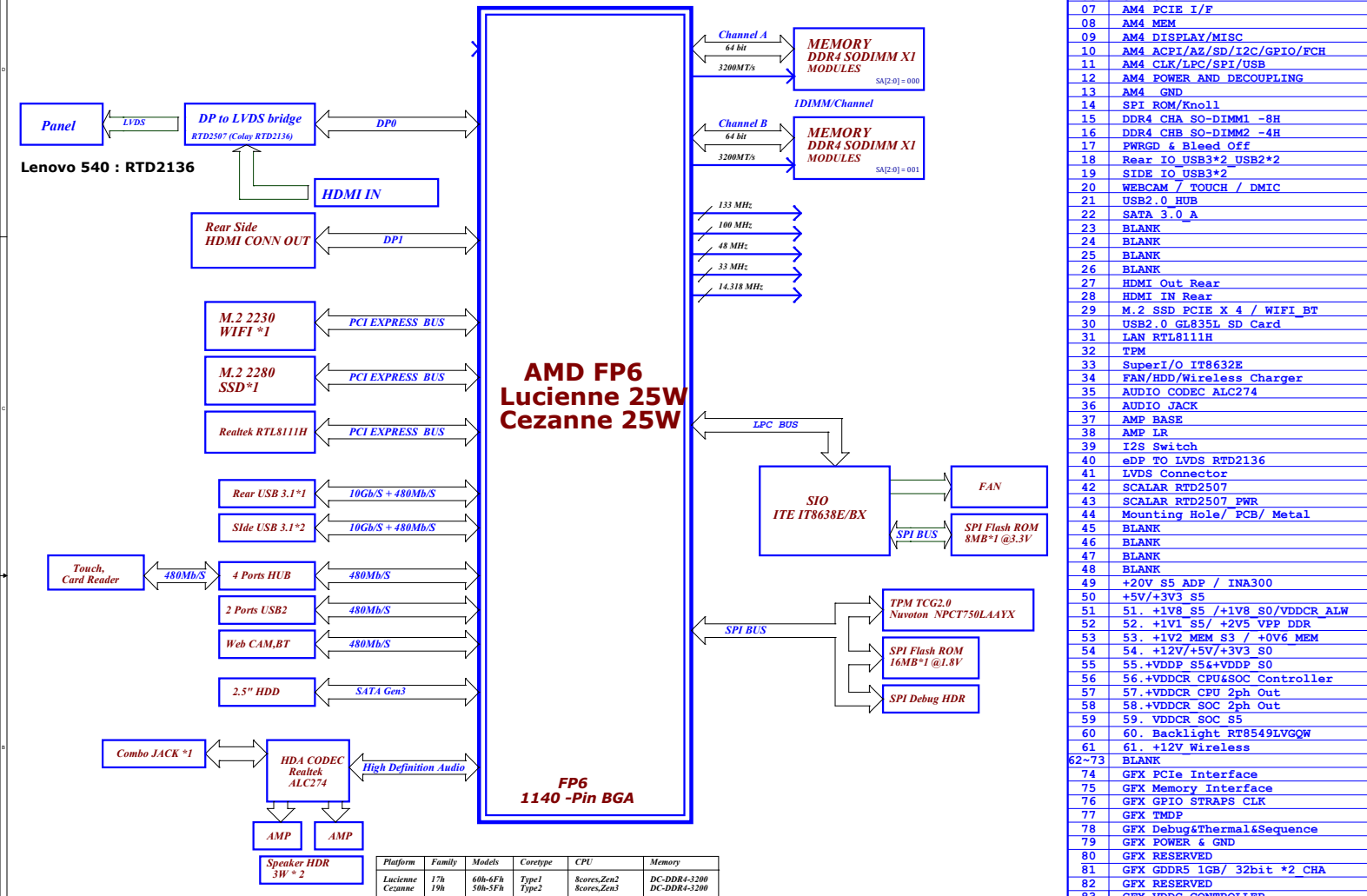


Project: AIO_560 AMD FP6

PCB Size : 310mm x 156mm x 1.2mm

Project A560-24ALC

Document No : X0.1



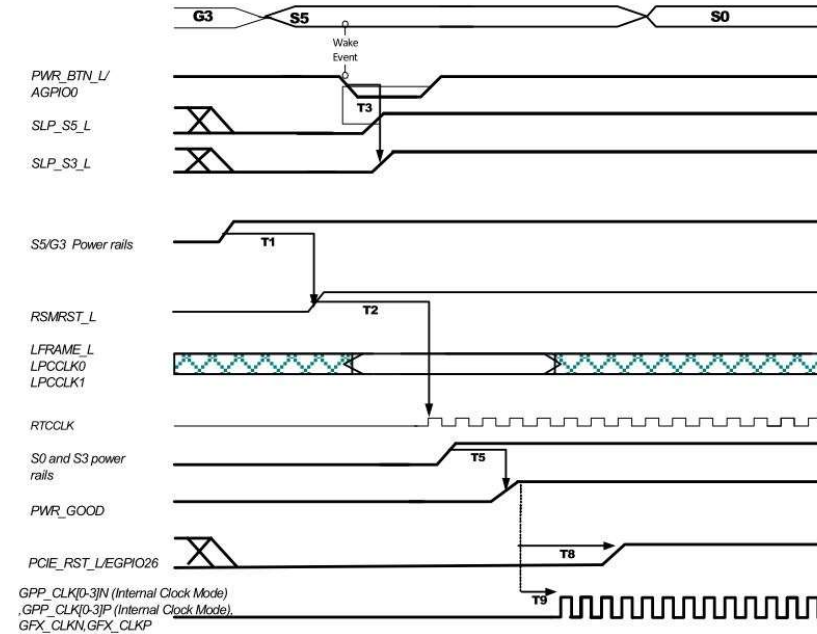
PAGE	TITLE
01	Block Diagram
02	Power Sequence
03	Power Delivery Map
04	RESET MAP
05	CLOCK DIAGRAM
06	SMBUS MAP
07	AM4 PCIE I/F
08	AM4 MEM
09	AM4 DISPLAY/MISC
10	AM4 ACPI/AZ/SD/I2C/GPIO/FCH
11	AM4 CLK/LPC/SPI/USB
12	AM4 POWER AND DECOUPLING
13	AM4_GND
14	SPI ROM/Knoll
15	DDR4 CHA SO-DIMM1 -8H
16	DDR4 CHB SO-DIMM2 -4H
17	PWRGD & Bleed Off
18	Rear IO USB3*2 USB2*2
19	SIDE IO USB3*2
20	WEBCAM / TOUCH / DMIC
21	USB2.0 HUB
22	SATA 3.0_A
23	BLANK
24	BLANK
25	BLANK
26	BLANK
27	HDMI Out Rear
28	HDMI IN Rear
29	M.2 SSD PCIE X 4 / WIFI_BT
30	USB2.0 GL835L SD Card
31	LAN RTL8111H
32	TPM
33	SuperI/O IT8632E
34	FAN/HDD/Wireless Charger
35	AUDIO CODEC ALC274
36	AUDIO JACK
37	AMP BASE
38	AMP LR
39	I2S Switch
40	eDP TO LVDS RTD2136
41	LVDS Connector
42	SCALAR RTD2507
43	SCALAR RTD2507_PWR
44	Mounting Hole/ PCB/ Metal
45	BLANK
46	BLANK
47	BLANK
48	BLANK
49	+20V S5 ADP / INA300
50	+5V/+3V3 S5
51	51. +1V8 S5 /+1V8 S0/VDDCR ALW
52	52. +1V1 S5/ +2V5 VPP DDR
53	53. +1V2 MEM S3 / +0V6 MEM
54	54. +12V/+5V/+3V3 S0
55	55.+VDDP S5+VDDP S0
56	56.+VDDCR CPU&SOC Controller
57	57.+VDDCR CPU 2ph Out
58	58.+VDDCR SOC 2ph Out
59	59. VDDCR SOC S5
60	60. Backlight RT8549LVGQW
61	61. +12V Wireless
62-73	BLANK
74	GFX PCIE Interface
75	GFX Memory Interface
76	GFX GPIO STRAPS CLK
77	GFX TMDP
78	GFX Debug&Thermal&Sequence
79	GFX POWER & GND
80	GFX RESERVED
81	GFX GDDR5 1GB/ 32bit *2 CHA
82	GFX RESERVED
83	GFX VDDC CONTROLLER
84	GFX VDDC Output
85	GFX +1V35 GPU DDR
86	GFX VDDCI Output
87	GFX +3V3 / GFX VDD 1.8
88	Strap Pin
89	GPIO Table
90	HSIO Port Map
91	EE Change List
92	BLANK
93	Power Board
94	DC IN

Table 41. Power Sequencing Group Definitions without Coin Cell Battery

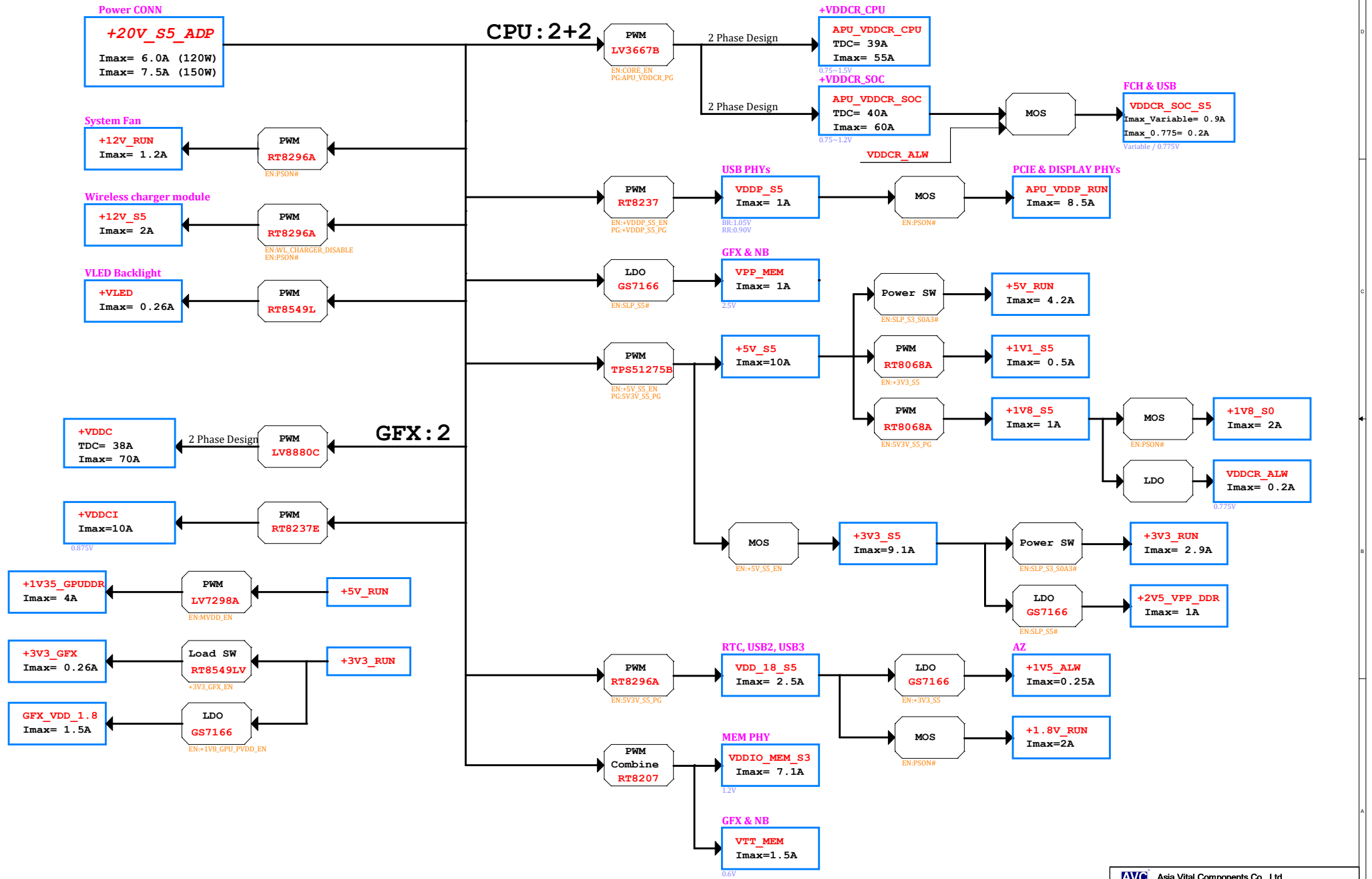
Group	System Power Domain	Voltages
Group A	G3/S5	VDDBT_RTC_G, VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5. The recommended power sequence for new designs is VDDP_S5 up to 90%, followed by VDD_18_S5, followed by VDD_33_S5.
Group B	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, and VDDP
Group C	S0	VDDCR_SOC, VDDCR_CPU** (AM4 only), VDDCR* (FP6 only)

Table 42. Power Sequencing Group Definitions with Coin Cell Battery

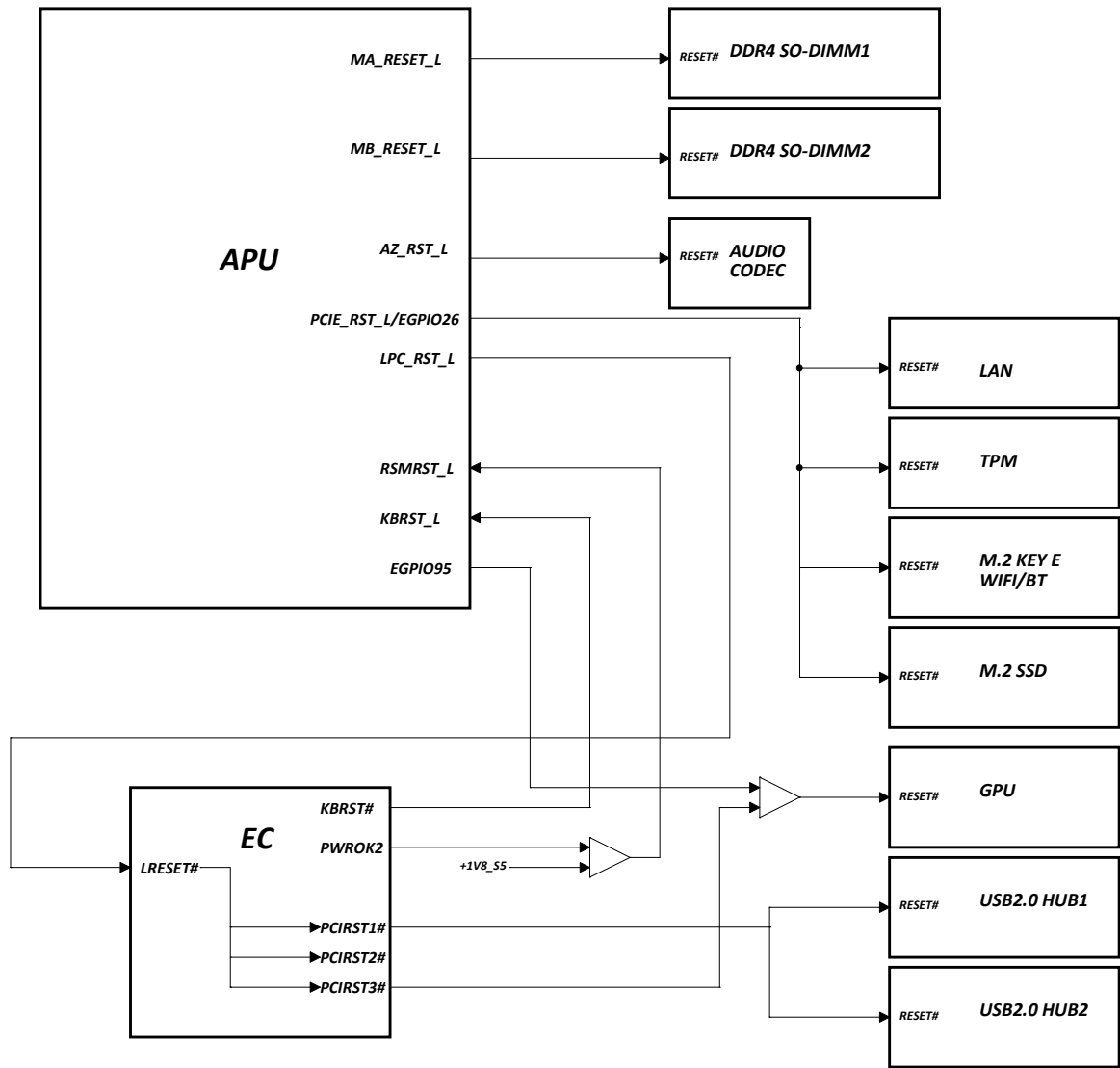
Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5. The recommended power sequence for new designs is VDDP_S5 up to 90%, followed by VDD_18_S5, followed by VDD_33_S5.
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, and VDDP
Group D	S0	VDDCR_SOC, VDDCR_CPU** (AM4 only), VDDCR* (FP6 only)



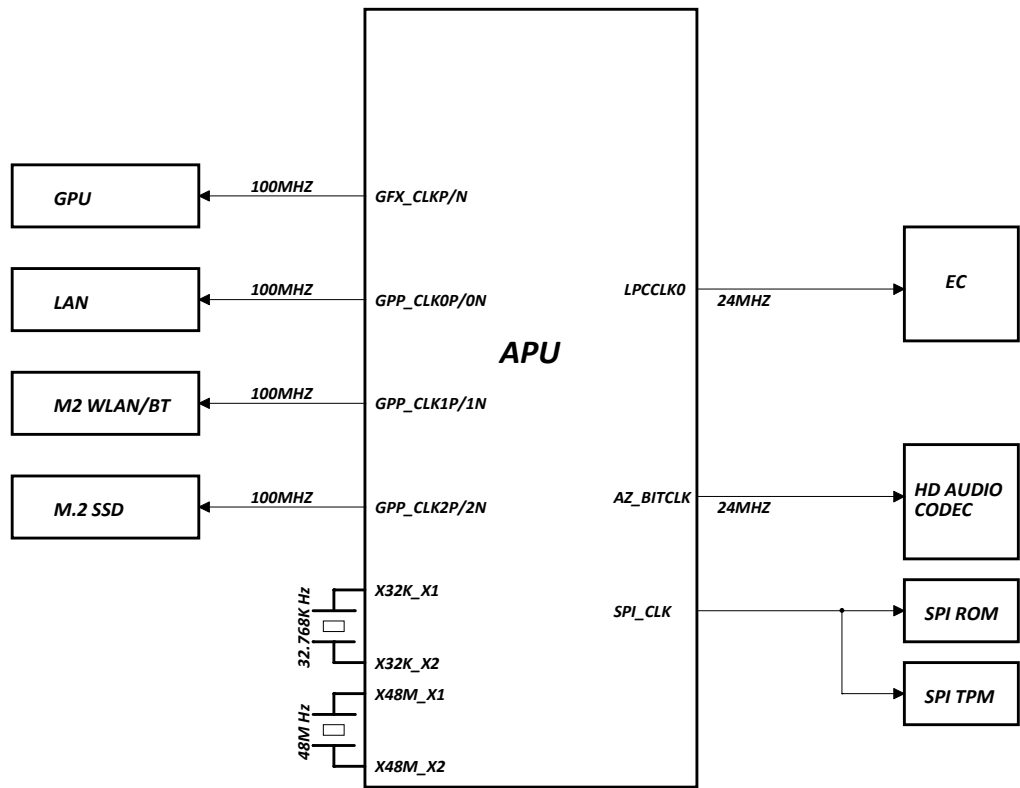
Power Map



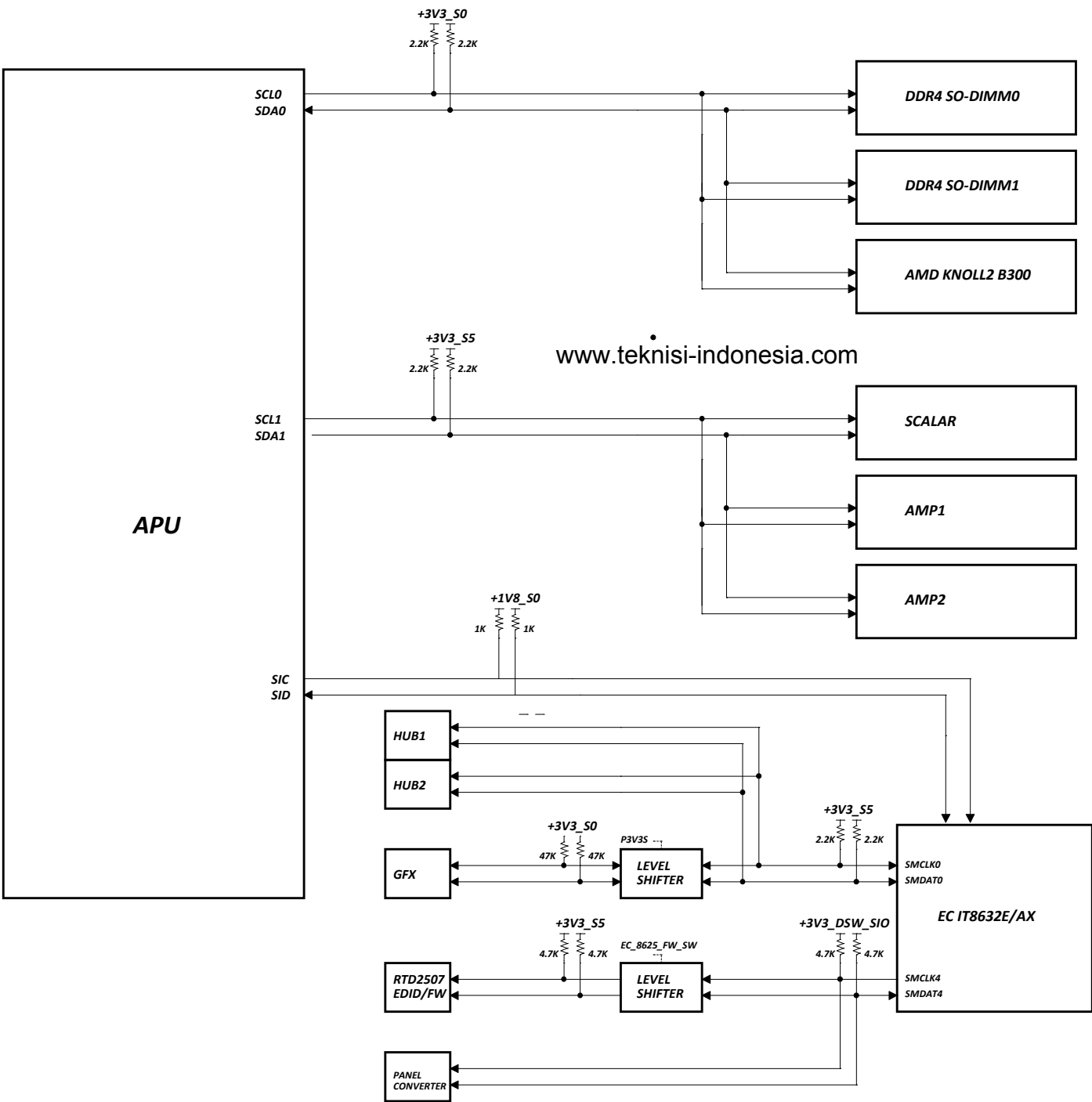
RST MAP



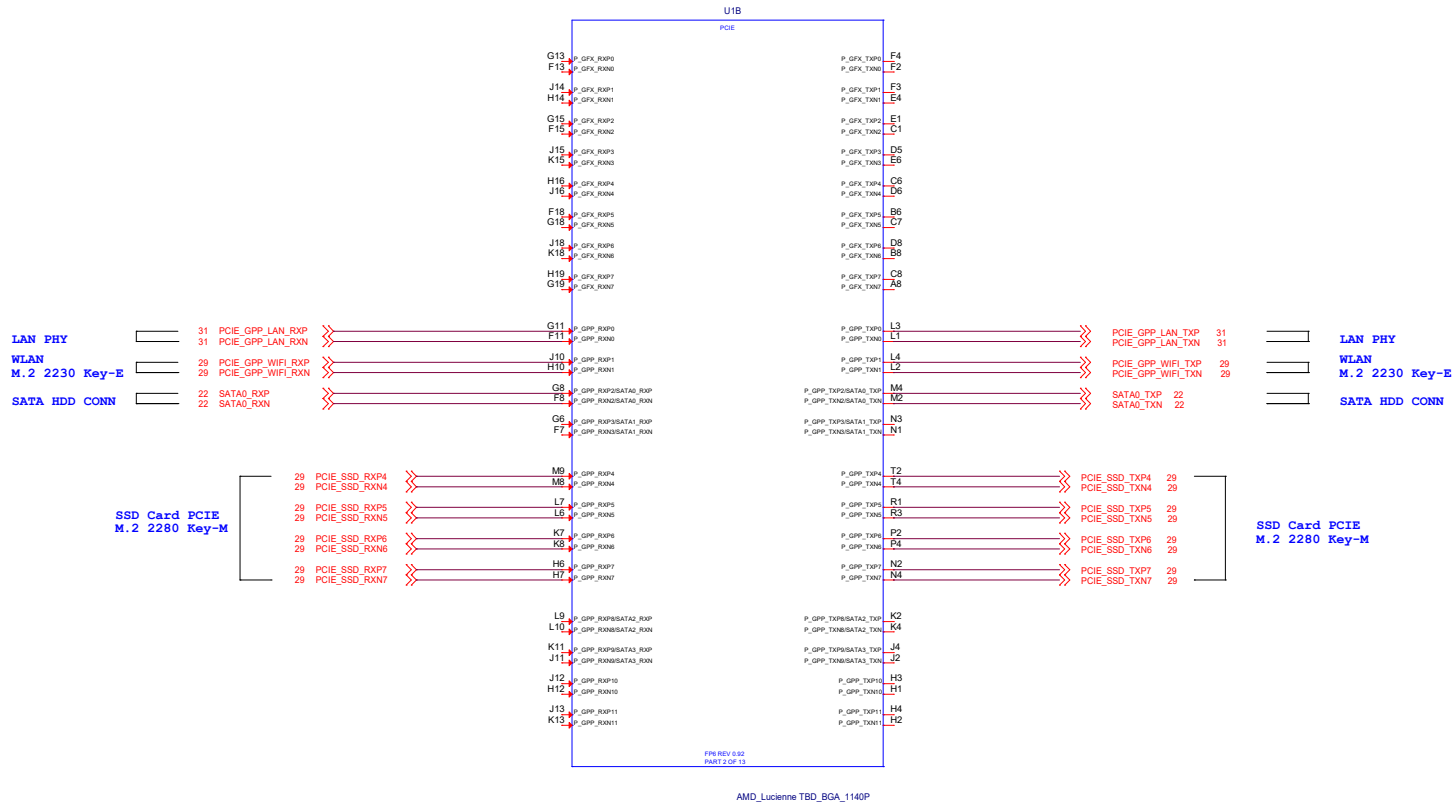
CLOCKS DIAGRAM

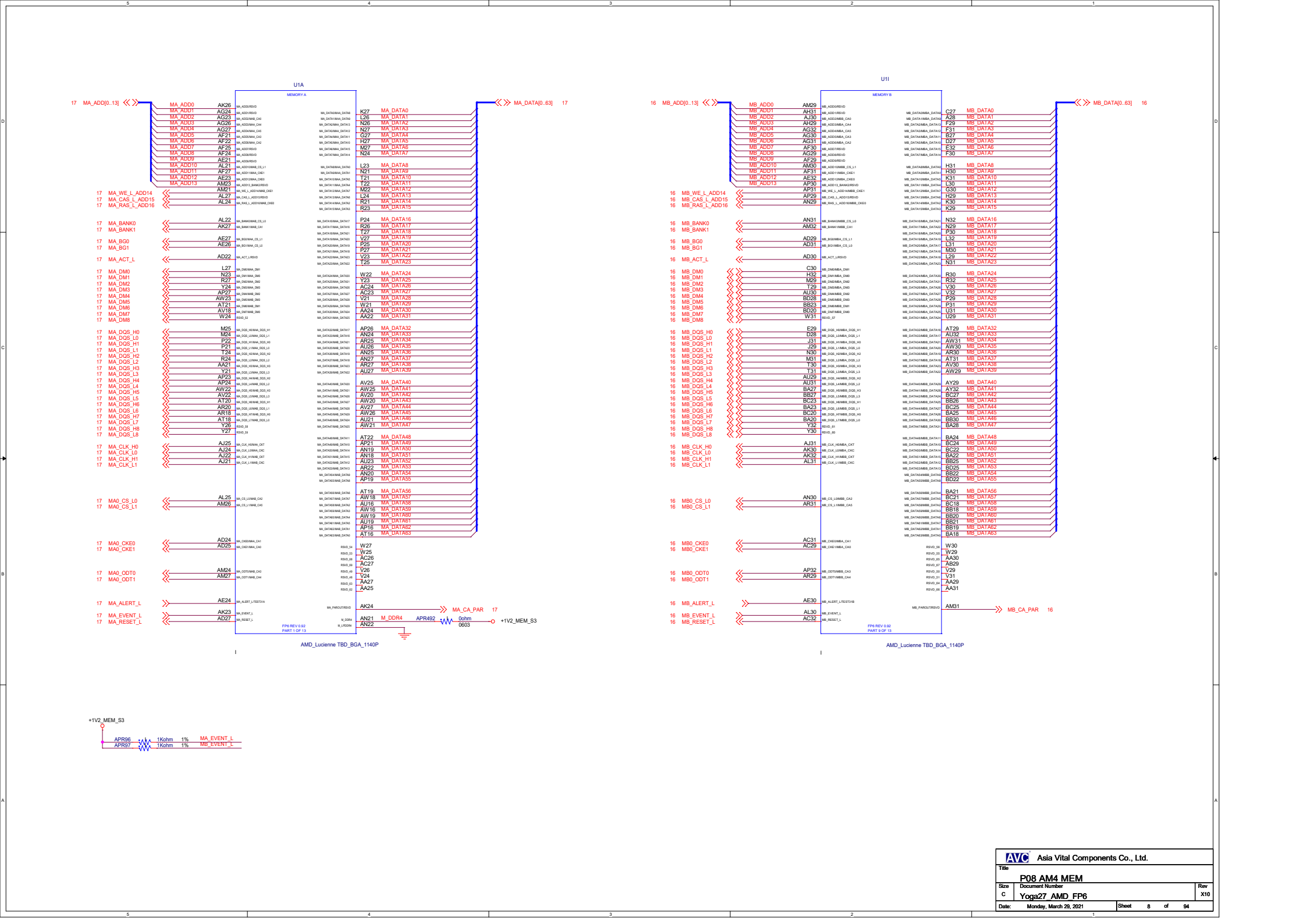


SMBus MAP

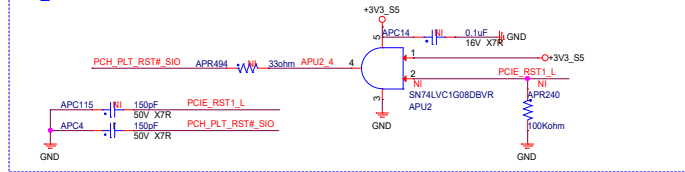


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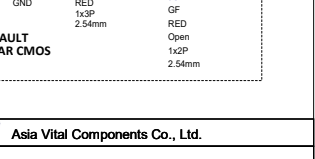
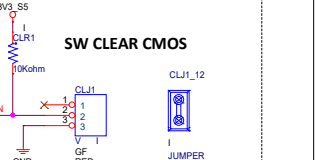
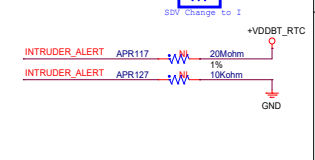
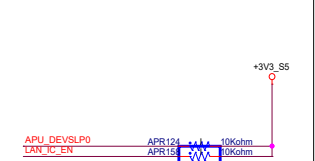
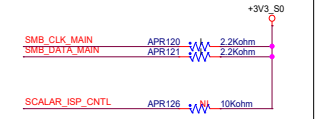
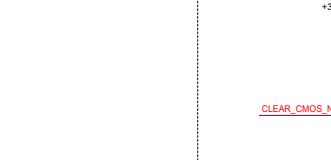
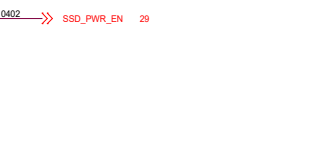
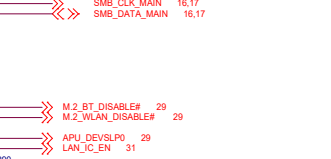
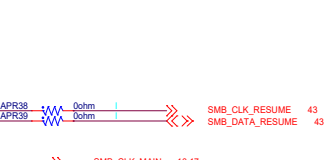
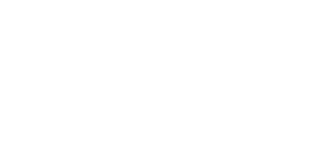
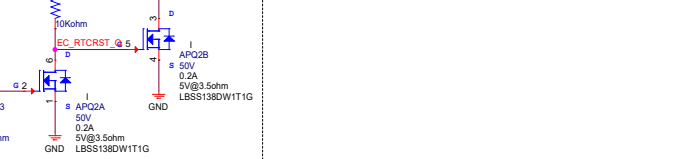
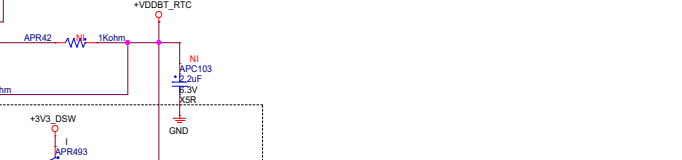
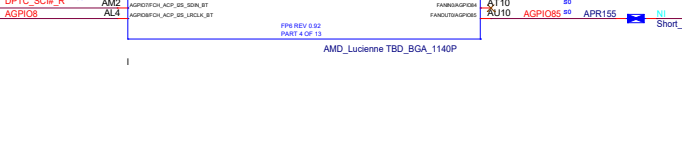
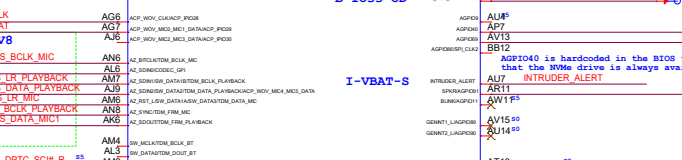
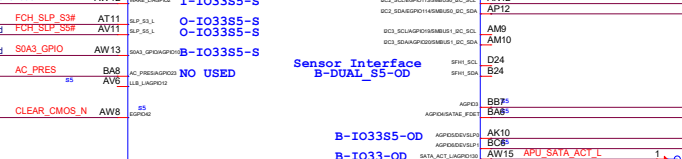
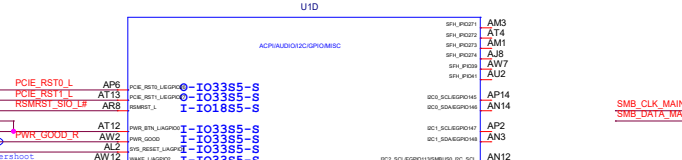
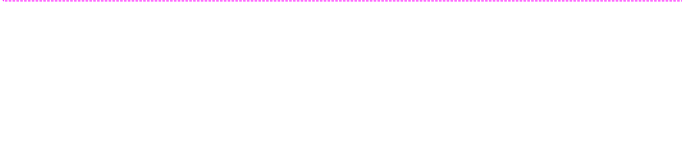
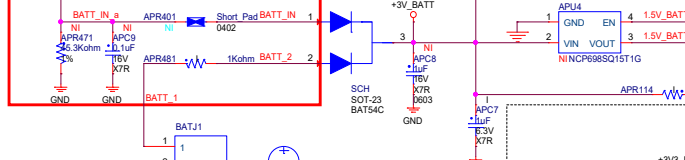
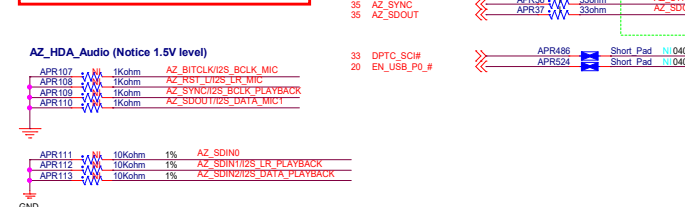
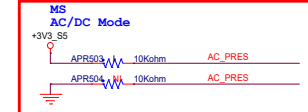
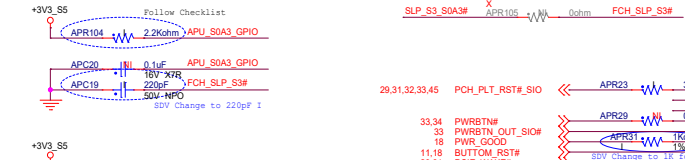
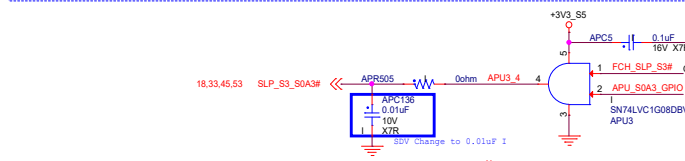
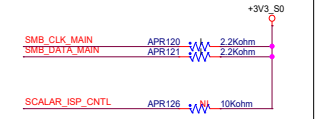
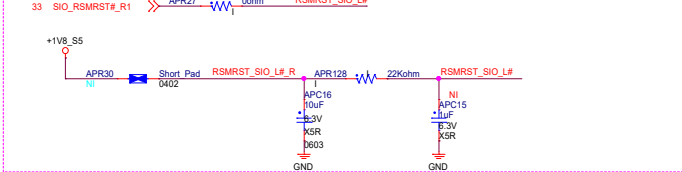




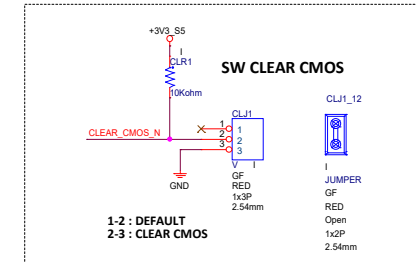
PCIE_RST# for PCIE device



RSMRST#



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USB3.1 Gen2 SIDE IO 1
USB3.1 Gen2 SIDE IO 2

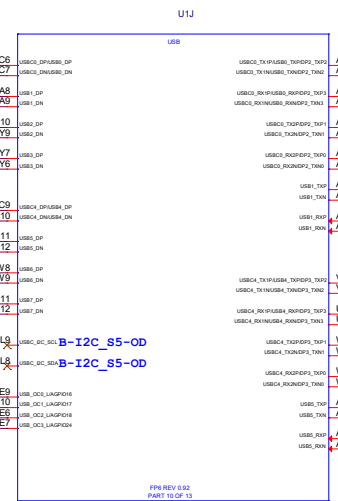
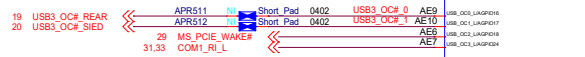
USB 2.0 REAR IO

Camera

USB3.1 Gen2 REAR IO

USB HUB

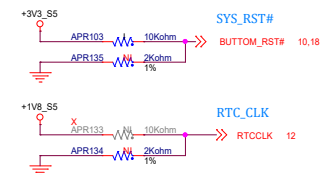
Touch



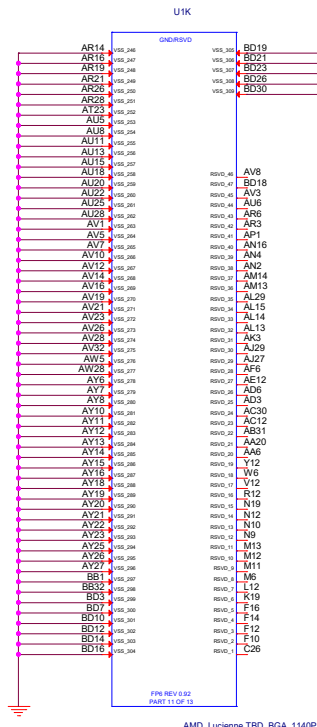
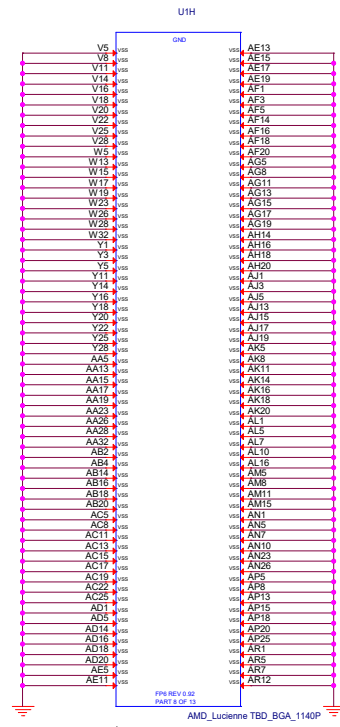
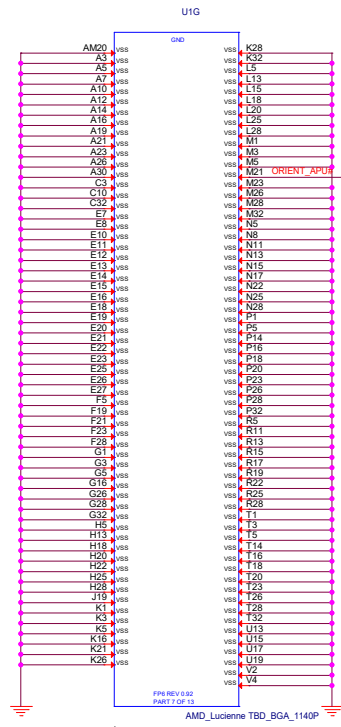
USB3.1 Gen2 SIDE IO 1

USB3.1 Gen2 SIDE IO 2

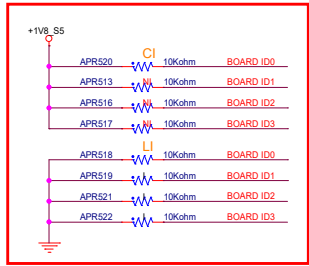
USB3.1 Gen2 REAR IO



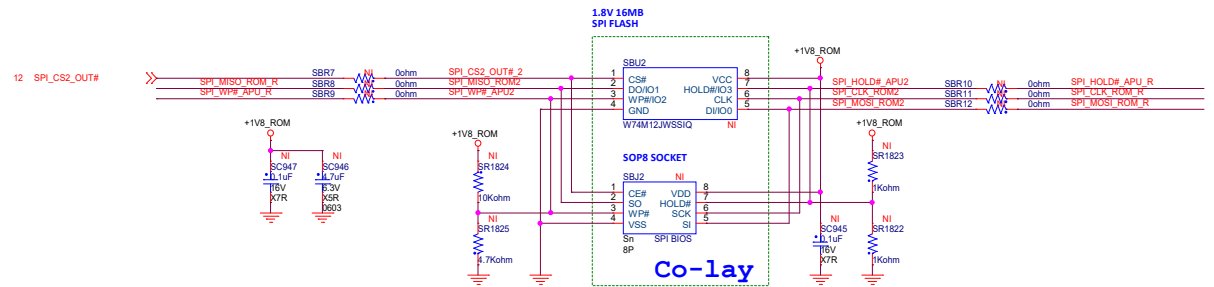
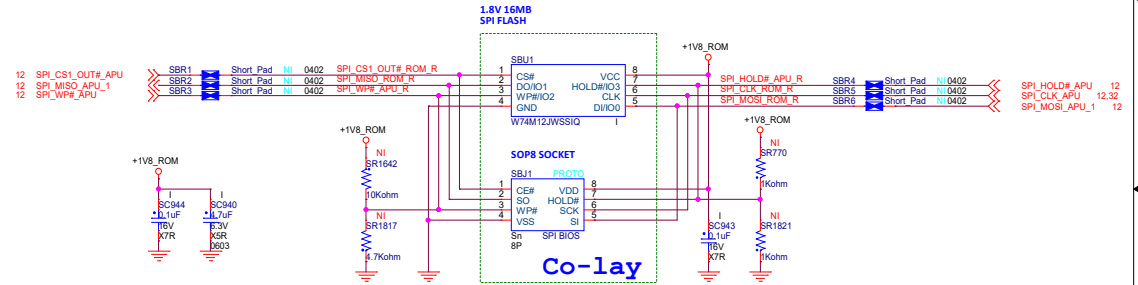
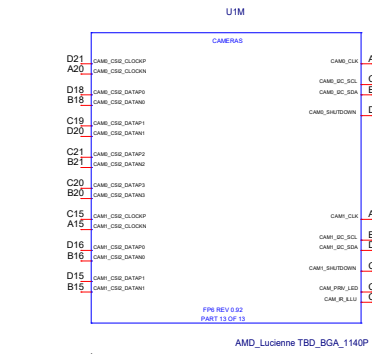
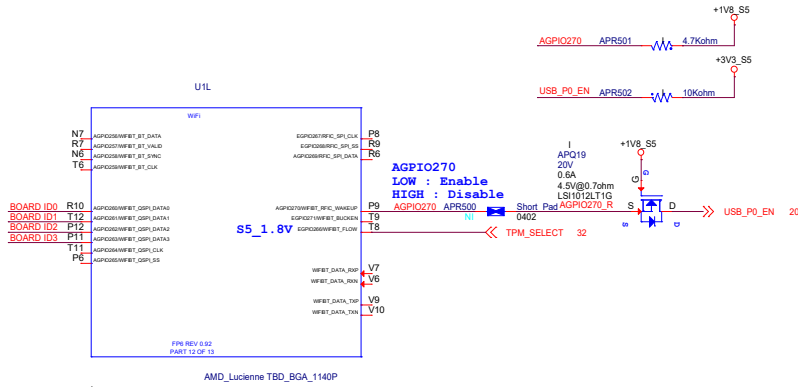
	SYS_RST#	SPI CLK	M_DDR4	M_LPDDR4
Pull High	1:NORMAL RESET MODE (DEFAULT)	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT)	Enable DDR4 memory controller 00 (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3	Disable LPDDR4x (need to have DDR4 enabled) 00 (± 5%) pull-down resistor or direct connect to VSS
Pull Low	0:SHORT RESET MODE	0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY	Disable DDR4 (need to have LPDDR4x enabled) 00 (± 5%) pull-down resistor or direct connect to VSS	Enable LPDDR4x memory controller 00 (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3

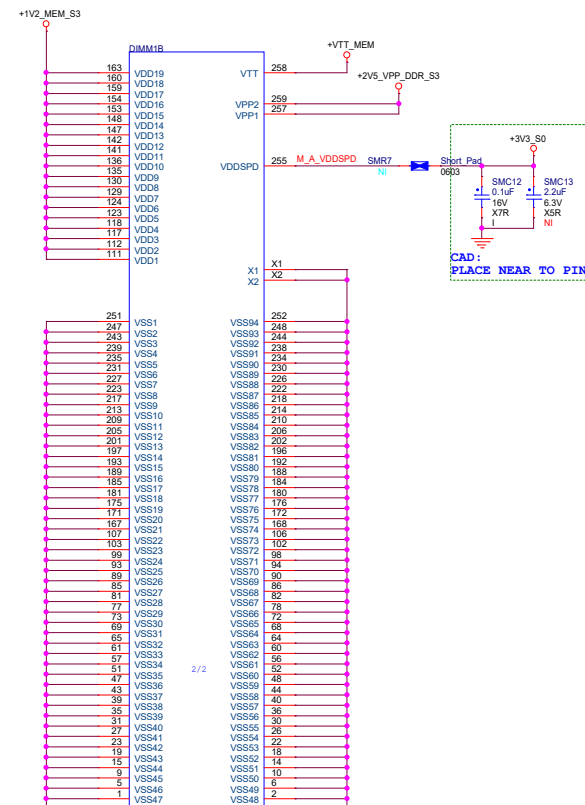
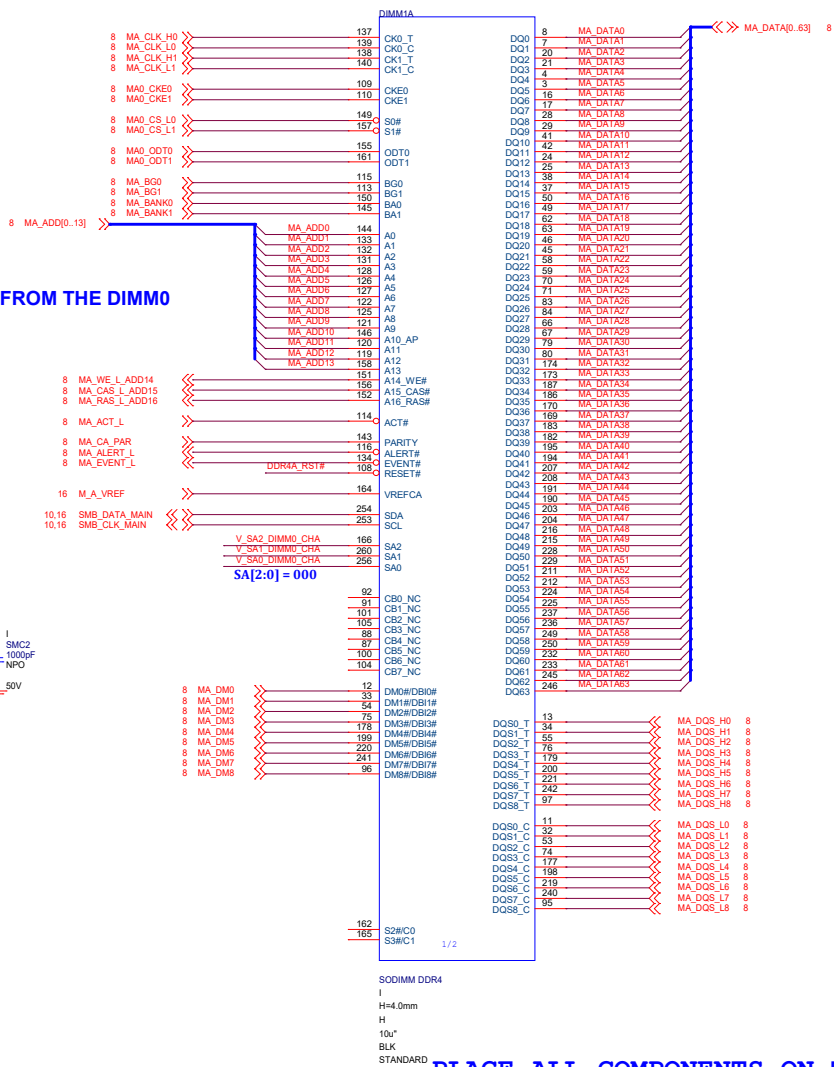
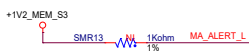
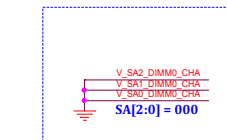
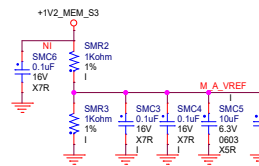
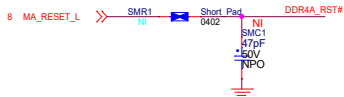


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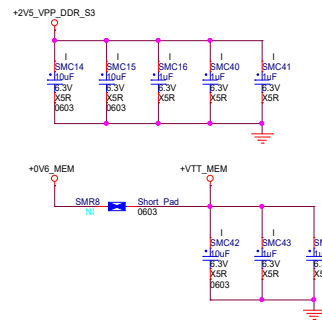
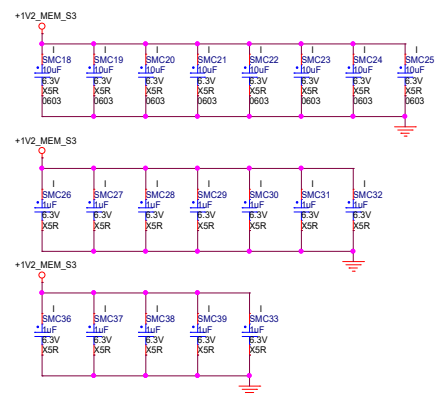


BOARD ID MAP	ID3	ID2	ID1	ID0
A560 24ALC Lucienne	0	0	0	0
A560 24ALC Cezanne	0	0	0	1

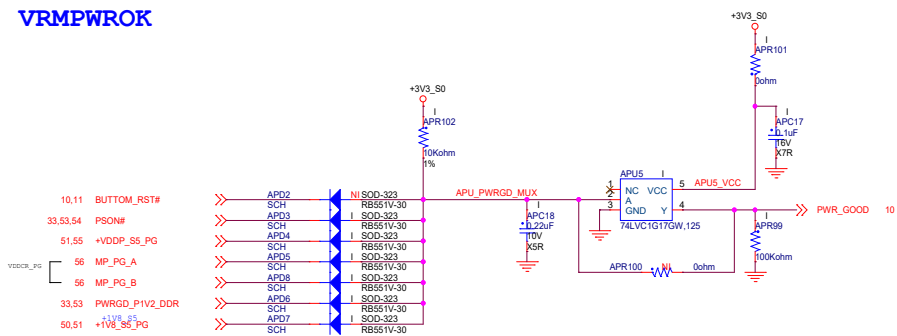




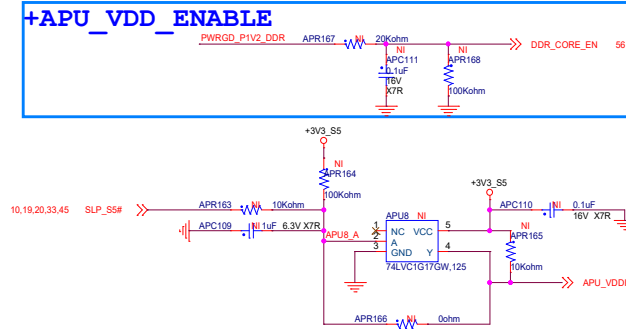
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VRMPWROK



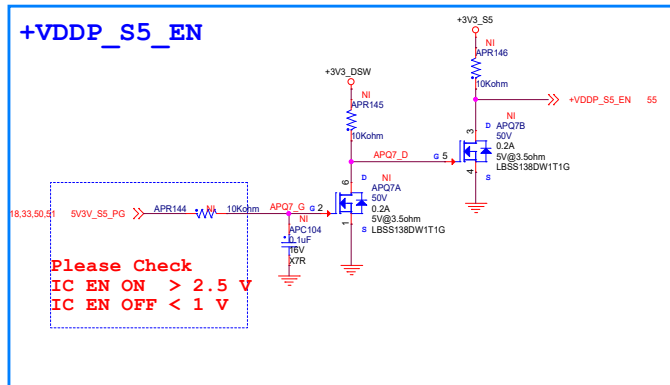
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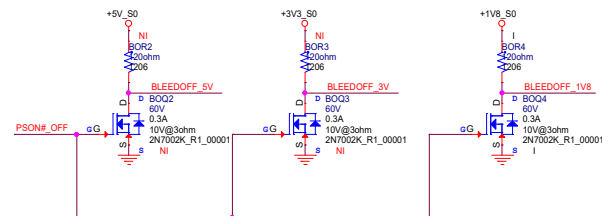
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5V3V_S5_PG APR523 0ohm +VDDP_S5_EN

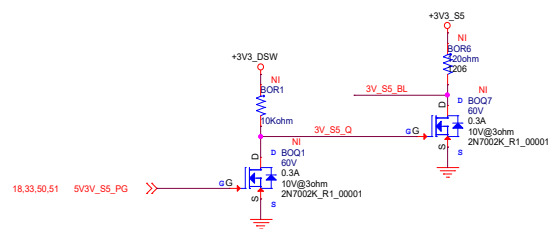
+VDDP_S5_EN



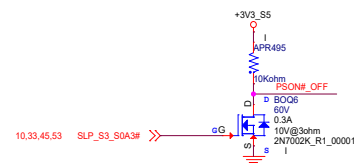
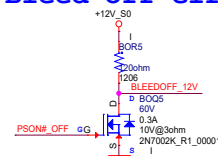
5V & 3.3V & 1.8V Bleed off circuit



5V_S5 and 3V_S5 Bleed off circuit



+12V Bleed off circuit



Asia Vital Components Co., Ltd.

Time

P20 PWRGD & Bleed Off

Size: C

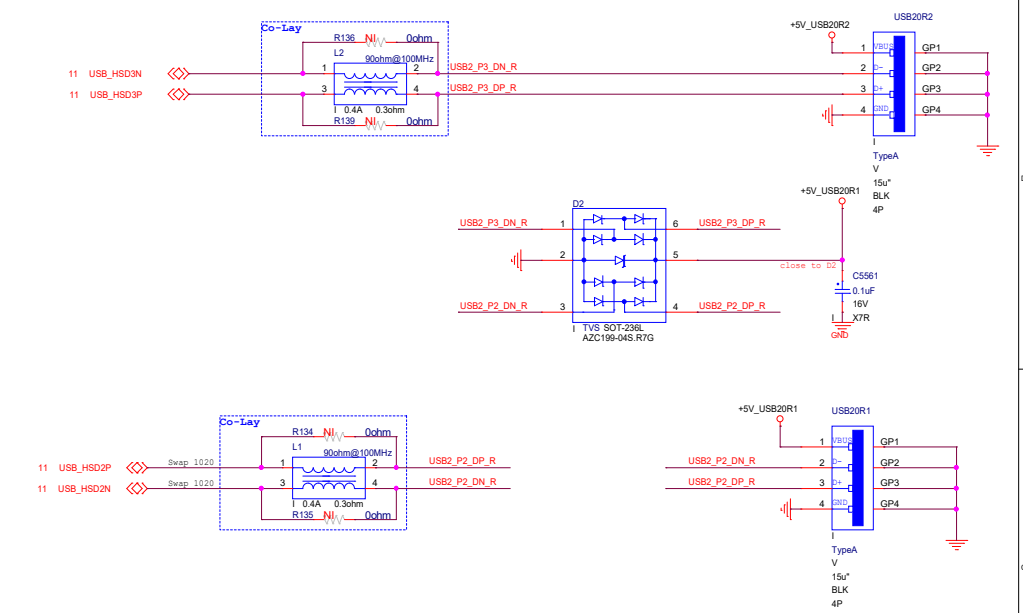
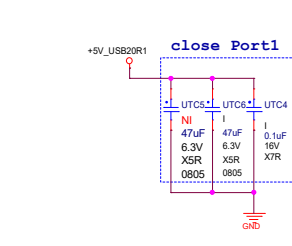
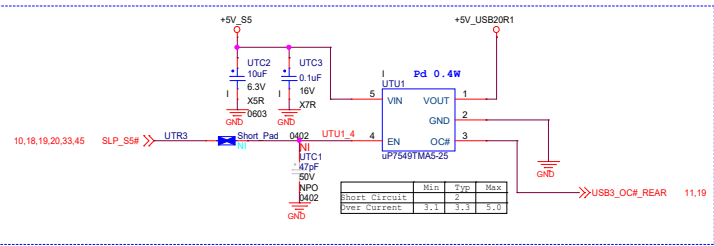
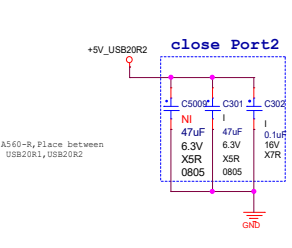
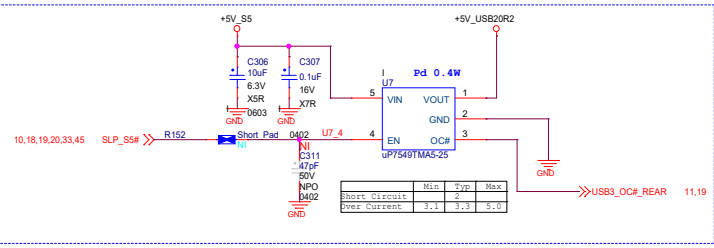
Docu: Yoda27_AMD_FP6

Date: Monday, March 29, 2021

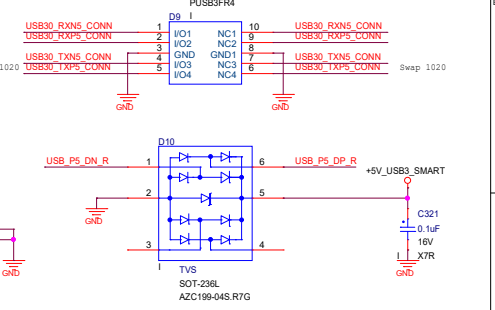
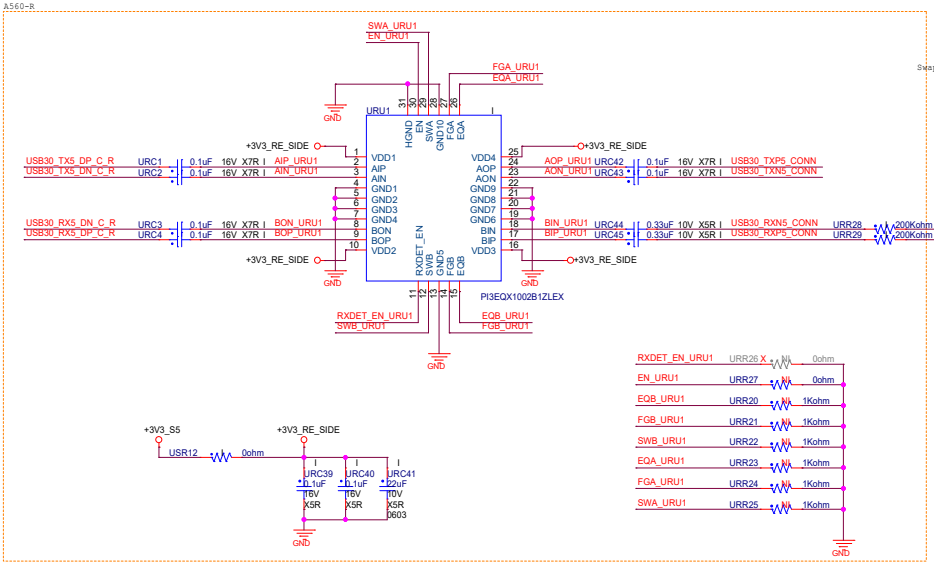
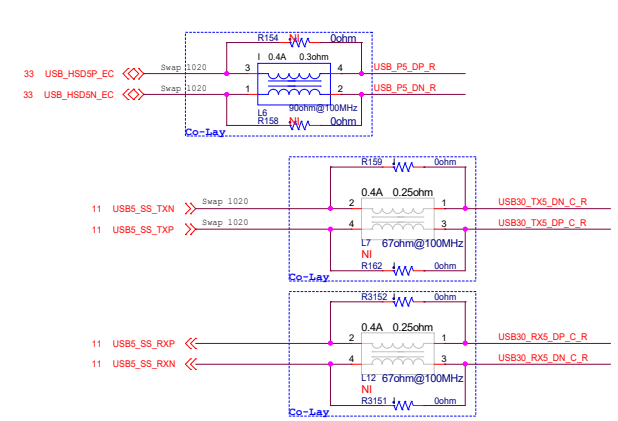
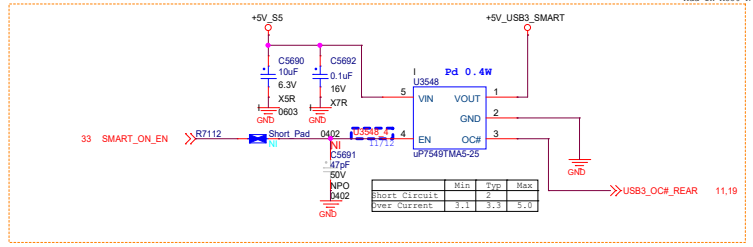
Rev: X10

Sheet: 18 of 94

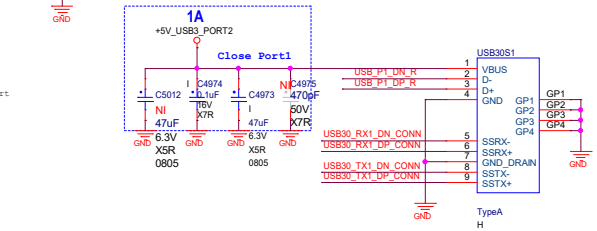
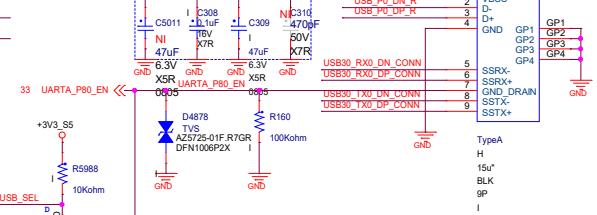
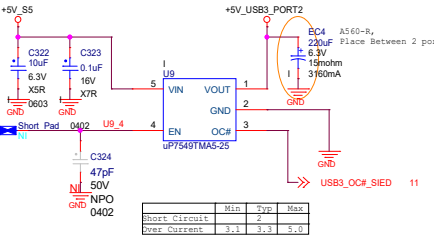
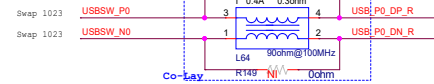
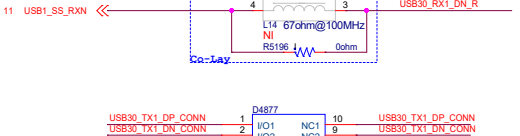
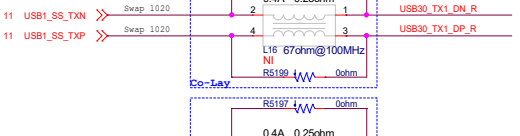
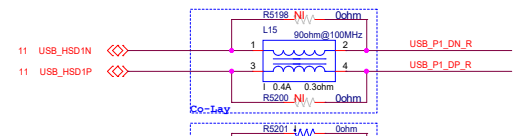
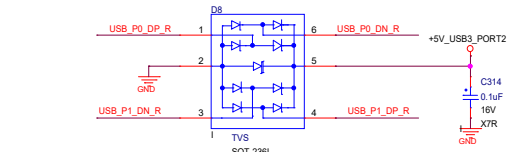
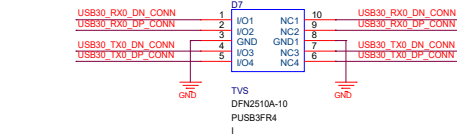
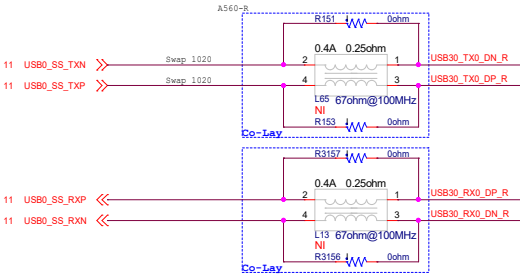
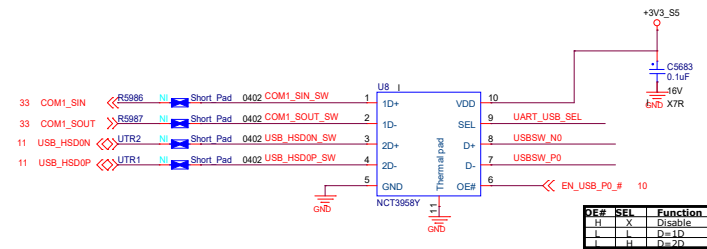
Rear USB20R1,USB20R2



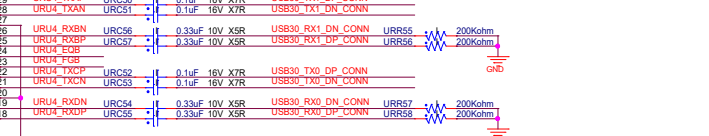
Rear USB31R1 Smart Power ON



Side IO USB3 *2

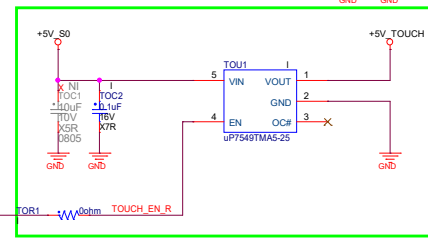
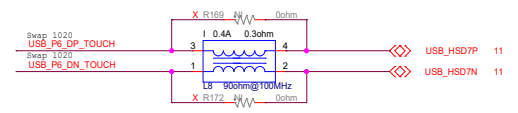
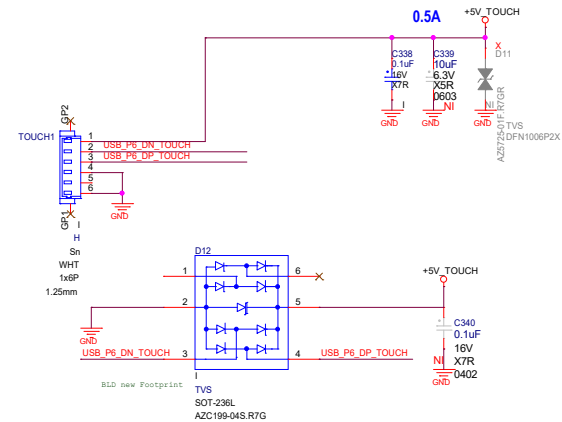


EQA/B/C/D Change to 68K
Vendor review(Follow YOGA)

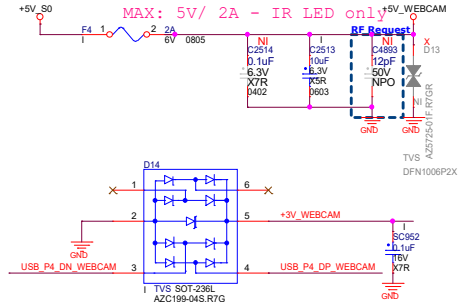


Touch

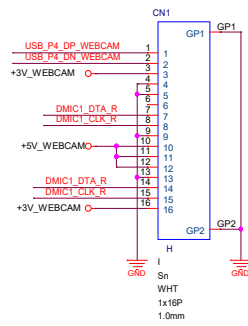
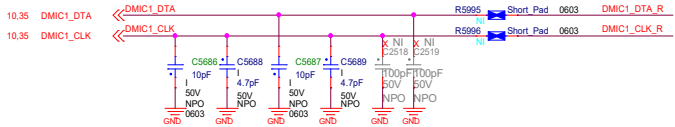
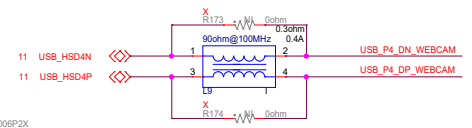
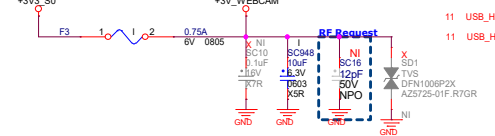
+5V_TOUCH
C341
12pF
50V
NPO
P402
GND



RGBIR / 2D Webcam

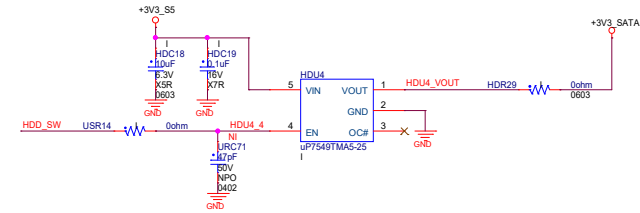
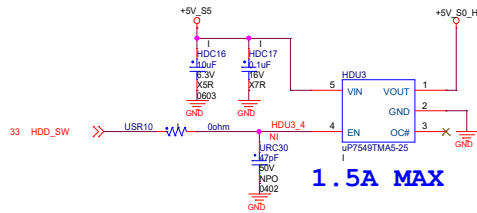


MAX : 3.3V/ 0.5A Camera



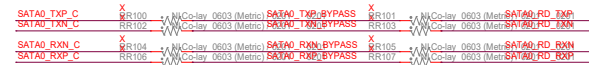
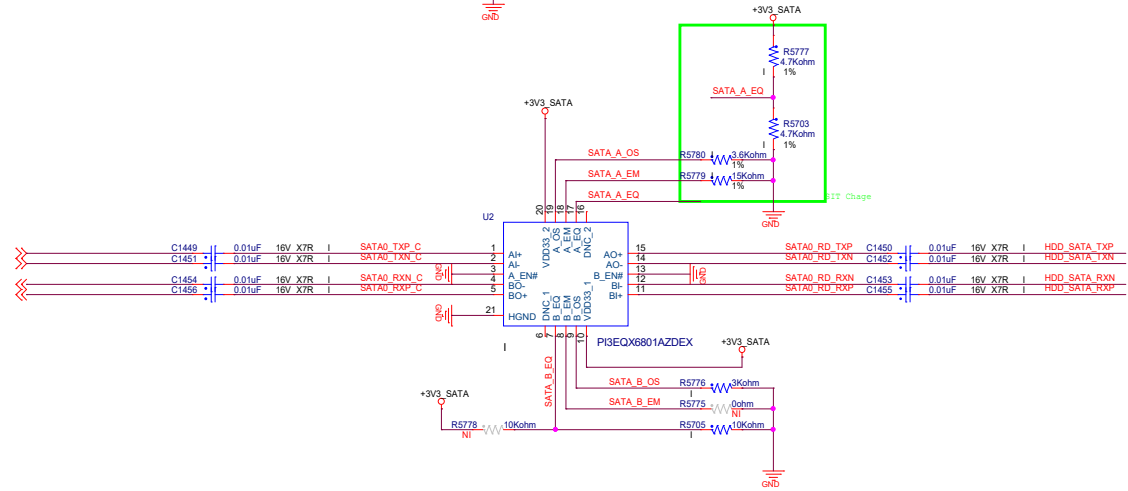
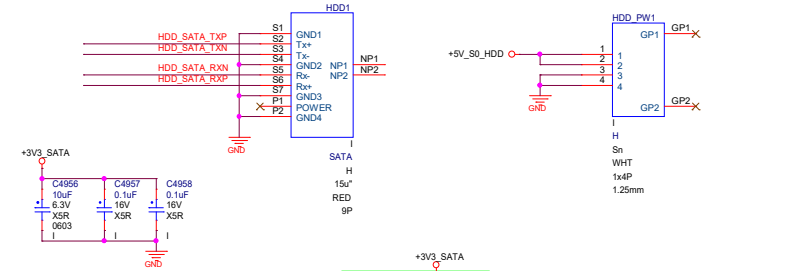
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2.5" HDD



7 SATA0_TXP
7 SATA0_TXN
7 SATA0_RXN
7 SATA0_RXP

SATA 3.0 CONN



COLAY with U2

PIN CONFIGURATION for CONTROL

PIN NAME	PIN FUNCTION DESCRIPTION	Control Configuration										
A_EN# B_EN#	With internal 200k-ohm pull-down resistor Low: Normal Operation High: Power Down Mode	For real application, they could be OPEN.										
A_EQ B_EQ	Input Equalization Tri-level Input	Equalization is controled by PIN7&PIN17 <table><tr><td colspan="2">Input Equalization for Channel A&B</td></tr><tr><td colspan="2">Input Equalization3.0Gb/s</td></tr><tr><td>0</td><td>8dB (A&B-CH)</td></tr><tr><td>1</td><td>16dB (A&B-CH)</td></tr><tr><td>Vdd/2</td><td>4dB (A&B-CH)</td></tr></table>	Input Equalization for Channel A&B		Input Equalization3.0Gb/s		0	8dB (A&B-CH)	1	16dB (A&B-CH)	Vdd/2	4dB (A&B-CH)
Input Equalization for Channel A&B												
Input Equalization3.0Gb/s												
0	8dB (A&B-CH)											
1	16dB (A&B-CH)											
Vdd/2	4dB (A&B-CH)											
A_EM B_EM	Output Emphasis Adjustment It is analog resistive adjustment. please refer to the next row table	Emphasis is controlled by PIN4&13, PIN5&12 and PIN6&11 of SW1 for Channel A, PIN4&13, PIN5&12 and PIN6&11 of SW2 for Channel B, <table><tr><td colspan="2">Pre-emphasis for Channel A&B</td></tr><tr><td>PIN4&13 is Open</td><td>0dB</td></tr><tr><td>PIN4&13 is short (14k RES)</td><td>+2.0dB</td></tr><tr><td>PIN5&12 is short (10k RES)</td><td>+3.0dB</td></tr><tr><td>PIN6&11 is short (6k RES)</td><td>+4.0dB</td></tr></table>	Pre-emphasis for Channel A&B		PIN4&13 is Open	0dB	PIN4&13 is short (14k RES)	+2.0dB	PIN5&12 is short (10k RES)	+3.0dB	PIN6&11 is short (6k RES)	+4.0dB
Pre-emphasis for Channel A&B												
PIN4&13 is Open	0dB											
PIN4&13 is short (14k RES)	+2.0dB											
PIN5&12 is short (10k RES)	+3.0dB											
PIN6&11 is short (6k RES)	+4.0dB											
A_OS B_OS	Output Swing Adjustment It is analog resistive adjustment. please refer to the next row table	Swing is controlled by PIN1&16, PIN2&15 and PIN3&14 of SW1 for Channel A, PIN1&16, PIN2&15 and PIN3&14 of SW2 for Channel B, <table><tr><td colspan="2">Swing Output for Channel A&B (mV, Vtx=diff-p at 6.0Gb/s)</td></tr><tr><td>PIN1&16 is short (5k RES)</td><td>660</td></tr><tr><td>PIN2&15 is short (4k RES)</td><td>820</td></tr><tr><td>PIN3&14 is short (2k RES)</td><td>1280</td></tr></table>	Swing Output for Channel A&B (mV, Vtx=diff-p at 6.0Gb/s)		PIN1&16 is short (5k RES)	660	PIN2&15 is short (4k RES)	820	PIN3&14 is short (2k RES)	1280		
Swing Output for Channel A&B (mV, Vtx=diff-p at 6.0Gb/s)												
PIN1&16 is short (5k RES)	660											
PIN2&15 is short (4k RES)	820											
PIN3&14 is short (2k RES)	1280											
PIN6&16 PIN10&20	Voltage PIN	PI3EQX6801AZDE (3.3V)@TQFN20: PIN10&20=VDD33 (3.3V), PIN6&16=DNC										

Receive Equalizer Configuration Table

x_EN#	x_EQ	Input Equalization @ 3.0GHz	Function
1	X	N/A	Channel x disabled. Hi-impedance terminations
0	0	8dB	Channel enabled, medium input equalization
0	1	16dB	Channel enabled, high input equalization
0	V _{DD} /2	4dB (Default)	Channel enabled, low input equalization

Output Swing Adjustment (1)

R[A:B]_OS (Ω)	Output Swing, mV (V _{TX-DIFF-p}) ⁽²⁾	
	3Gbps	6Gbps
5.5K	450	600
5K	490	660
4.5K	540	730
4K	600	820
3.5K	670	910
3K	760	1,000
2.5K	870	1,080
2K	990	1,200

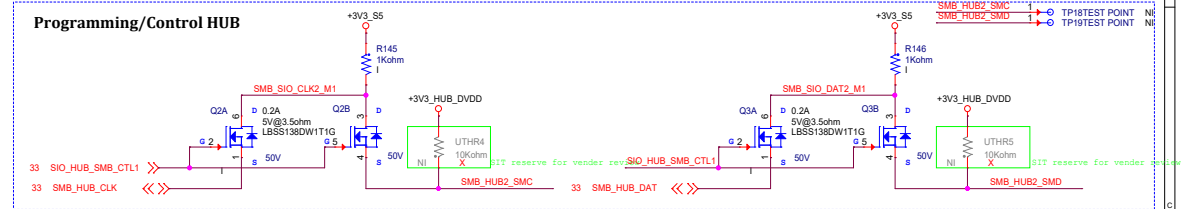
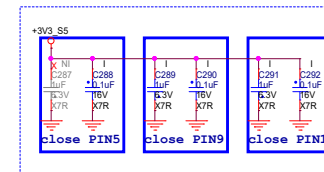
Note:
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Auto HDD Rate Detection is ON.

Output Emphasis Adjustment (1, 2)

R[A:B]_EM (Ω)	Pre-emphasis
Do Not Connect	0dB
14K	+2.0dB
10K	+3.0dB
6K	+4.0dB
2K	+6.0dB

Note:
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Referenced to output saving of 600mV, will vary as a function of swing, increasing as swing decreases.

Note:
V_{MAX} of output can not exceed 1,200mVpp (i.e. V_{DIFF-PRE} can not exceed 1,200mV)



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Size	Document Number	Rev
C	AIO-540_AMD_AM4	V1.0
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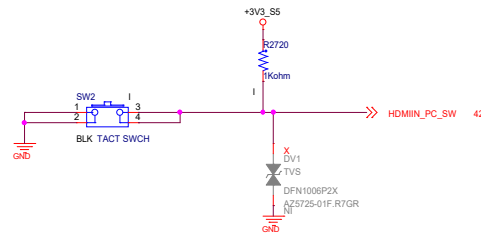
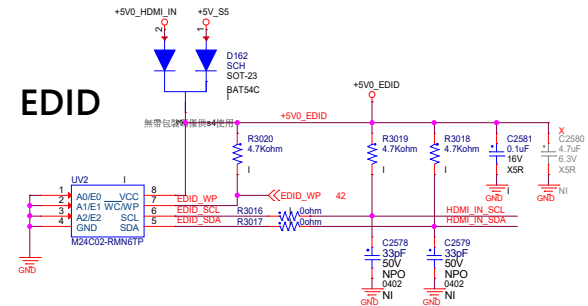
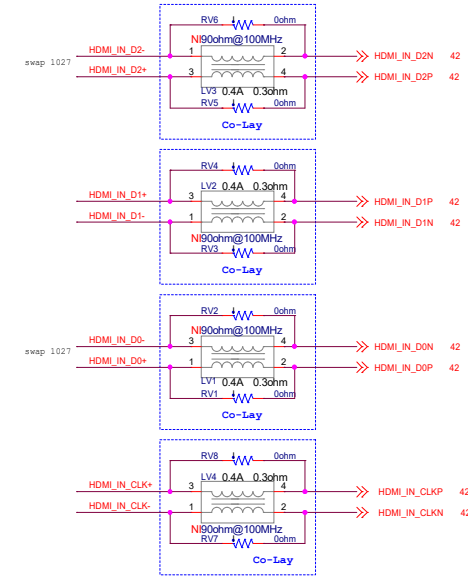
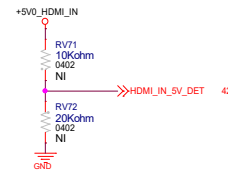
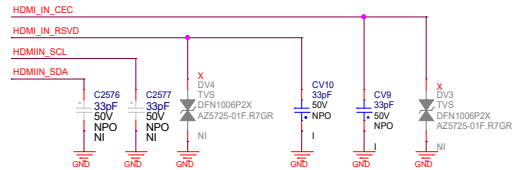
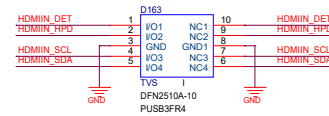
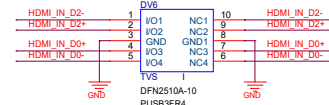
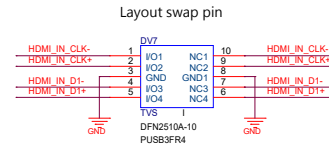
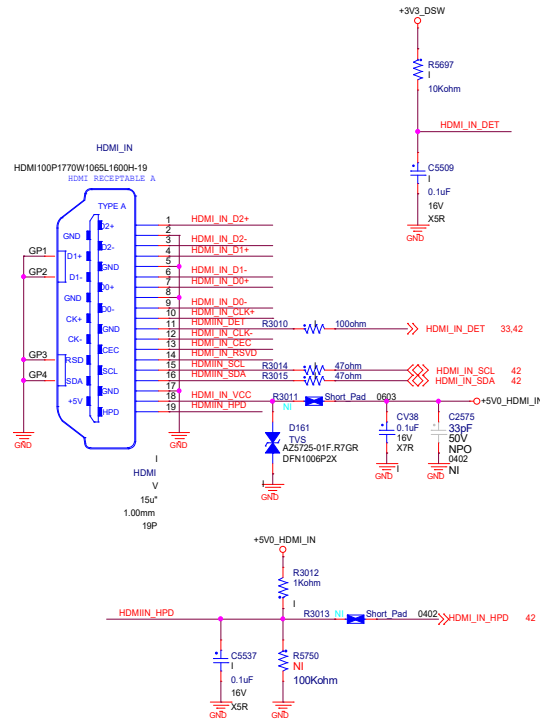
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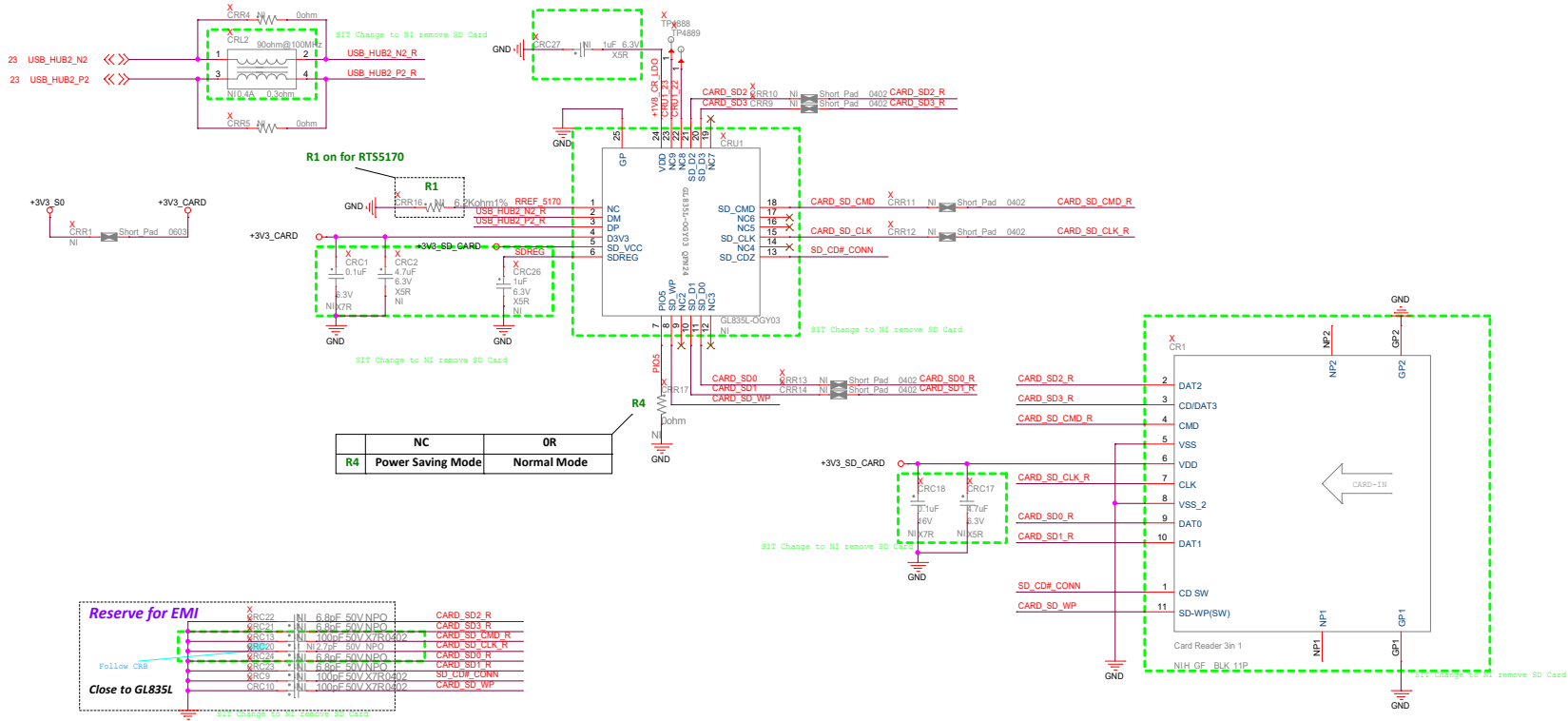
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PCIe Redriver WIFI		
Size	Document Number	Rev
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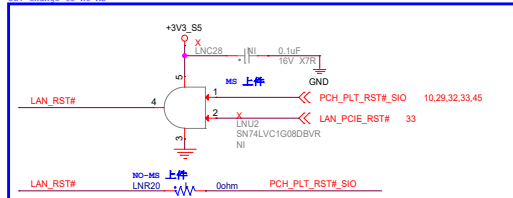
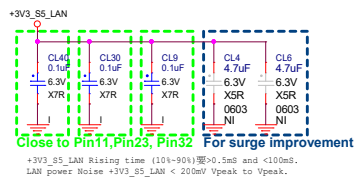
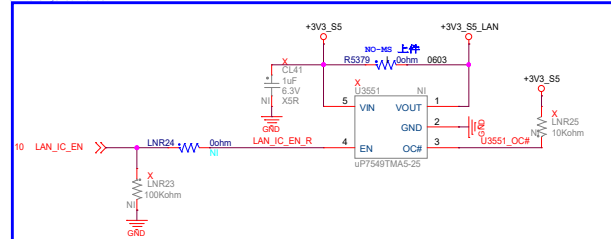
HDMI IN



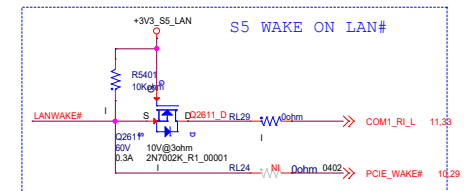
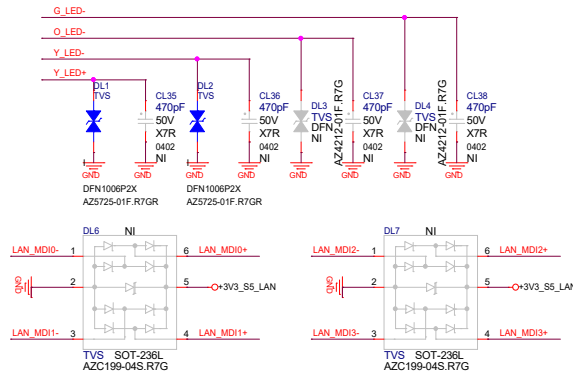
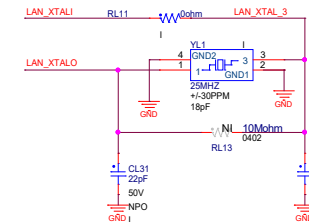
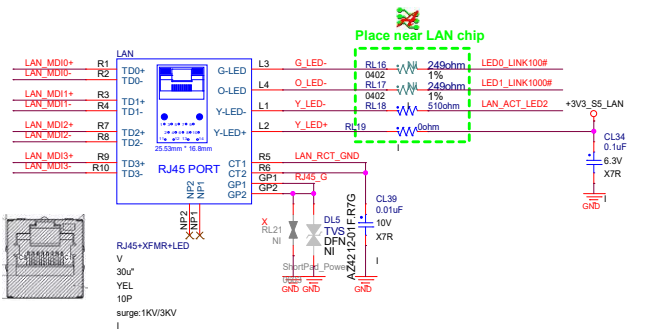
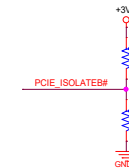
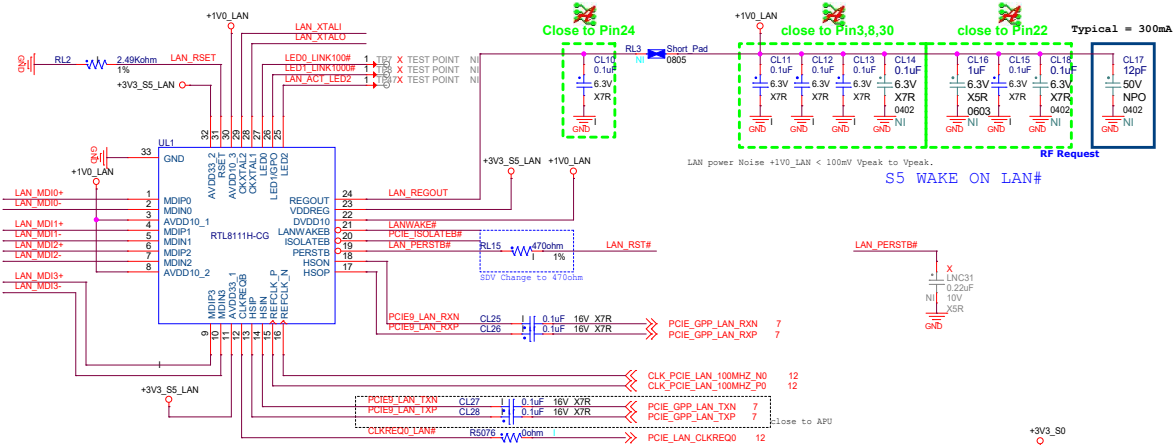
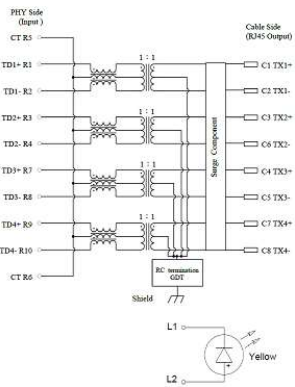
CARD READER GL835L



LAN RTL8111H-CG/ RJ45 CONN



WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M_inactive	
on	10M_active	
on	100M_inactive	
on	100M_active	
on	1G_inactive	
on	1G_active	



Must select low C_{ISS} MOSFET <30pF.

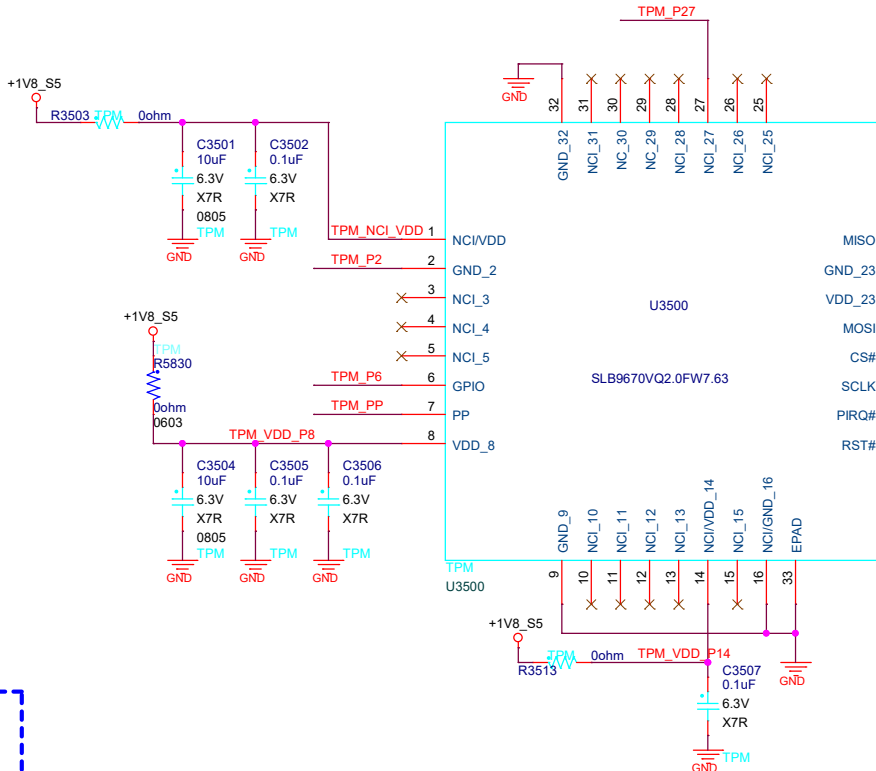
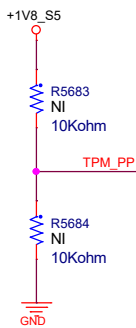
To PCH GPIO

15 TPM_SELECT

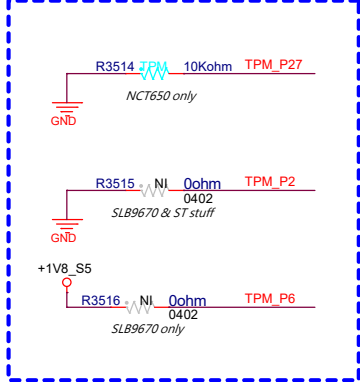


TPM_SELECT	TYPE
H	HW TPM
L	FW TPM

TPM 2.0

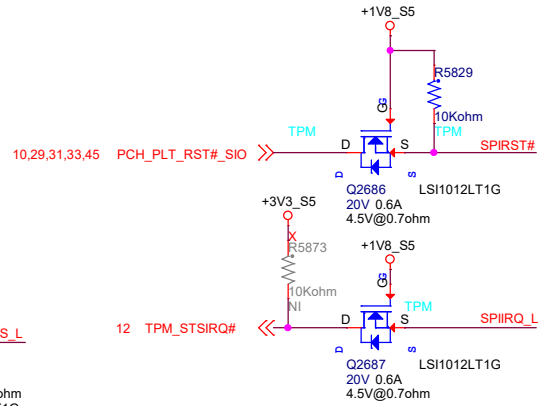
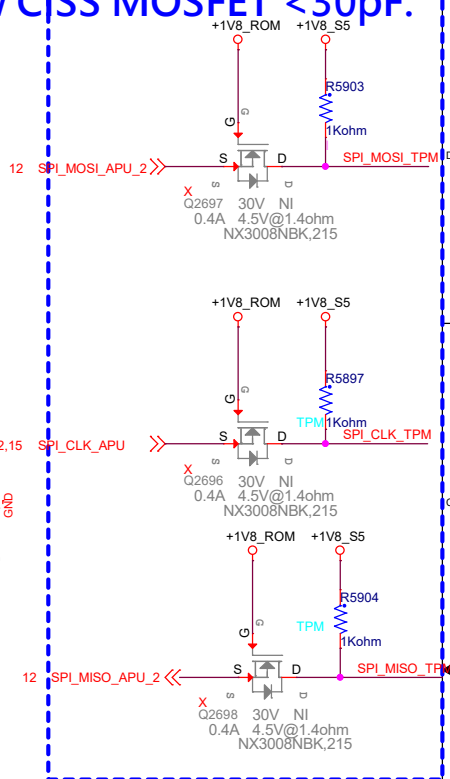
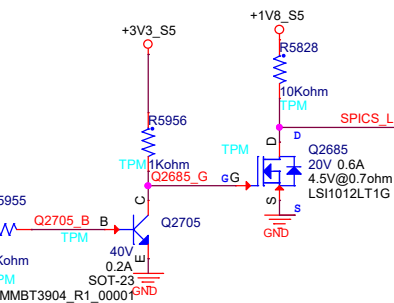


Co-lay option

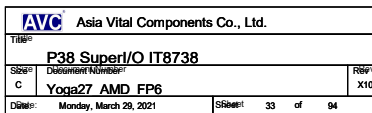


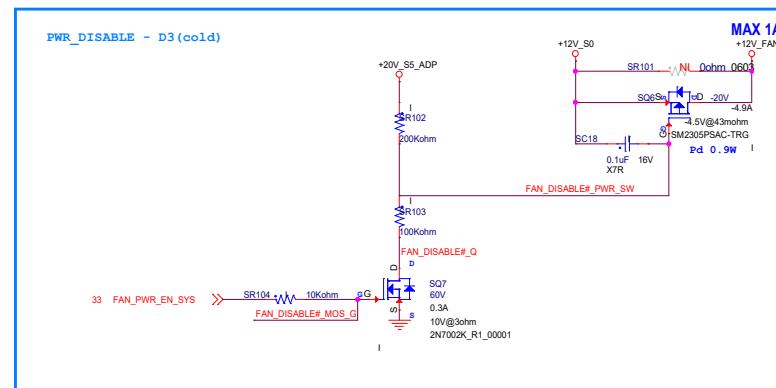
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TPM_P27	V		
TPM_P2		V	V
TPM_P6		V	

Win10 RS2 logo: ST33HTPH2E32AHA6
Win10 RS3 logo: ST33TPHF2ESPI

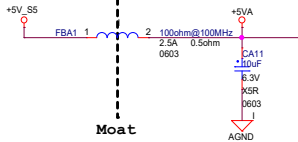


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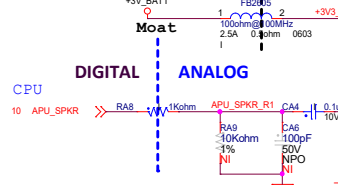




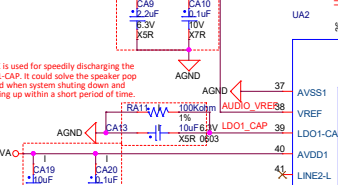
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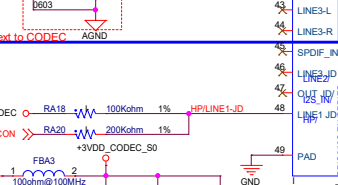
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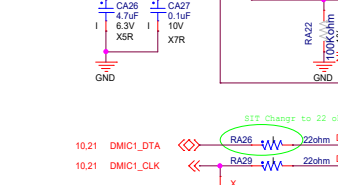
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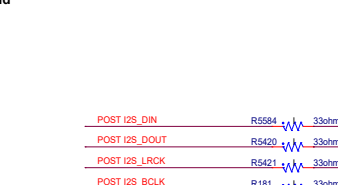
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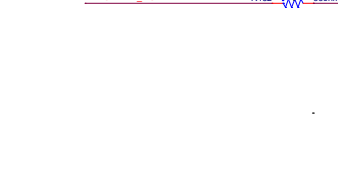
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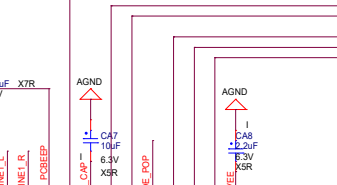
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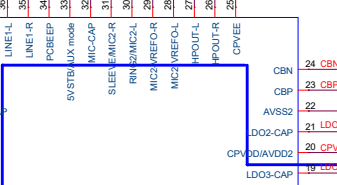
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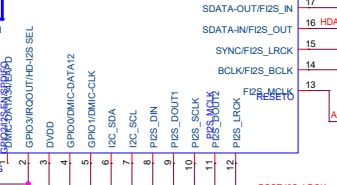
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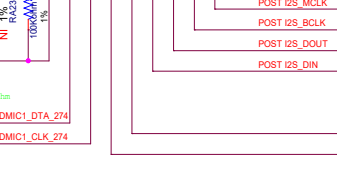
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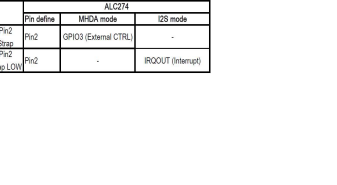
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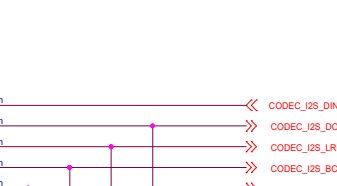
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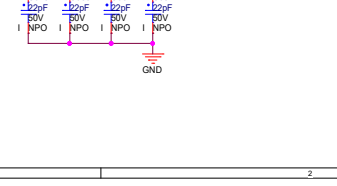
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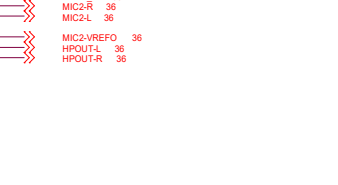
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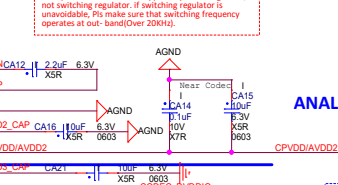
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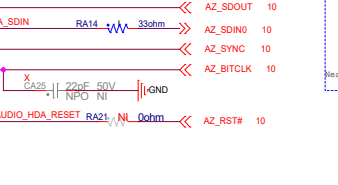
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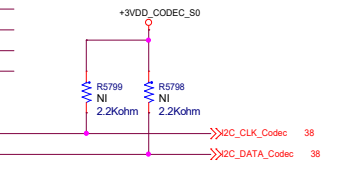
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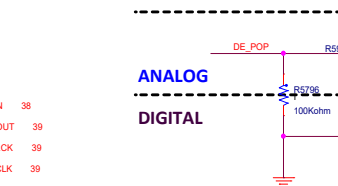
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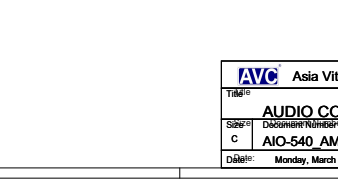
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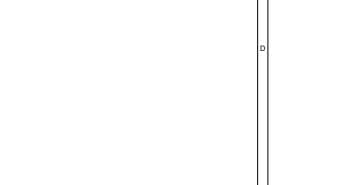
DIGITAL ANALOG



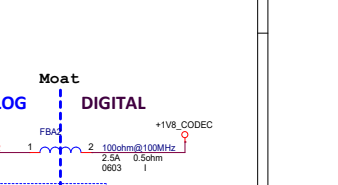
DIGITAL ANALOG



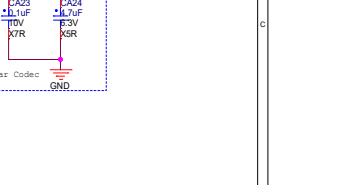
DIGITAL ANALOG



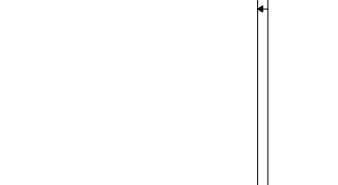
DIGITAL ANALOG



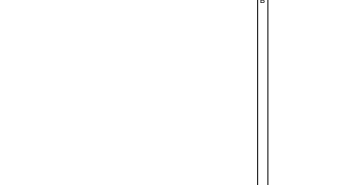
DIGITAL ANALOG



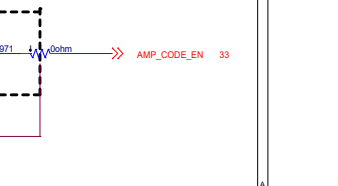
DIGITAL ANALOG



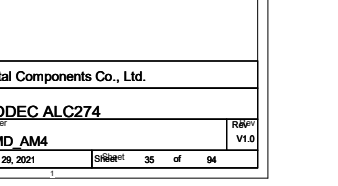
DIGITAL ANALOG



DIGITAL ANALOG



DIGITAL ANALOG



AVC Asia Vital Components Co., Ltd.

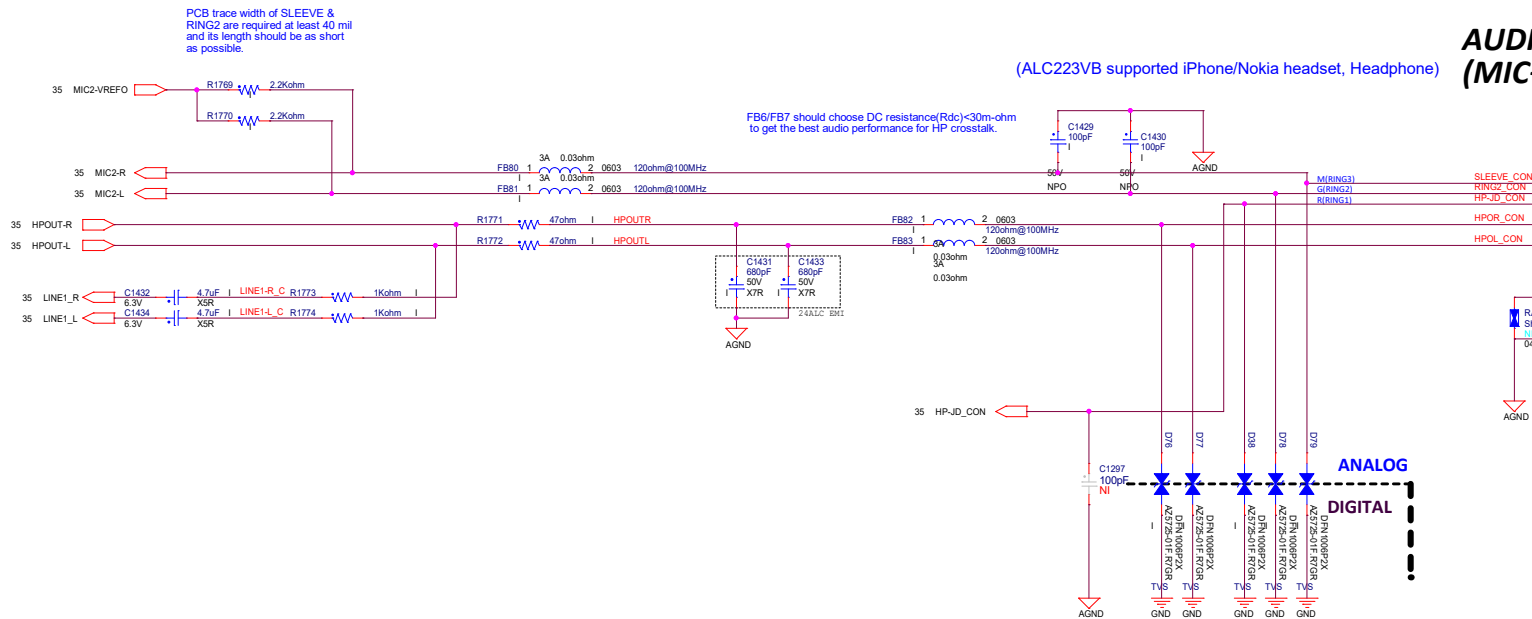
TIME

Size: AUDIO CODEC ALC274

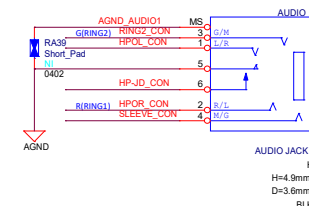
C: AIO-540_AMD_AM4

Date: Monday, March 29, 2021

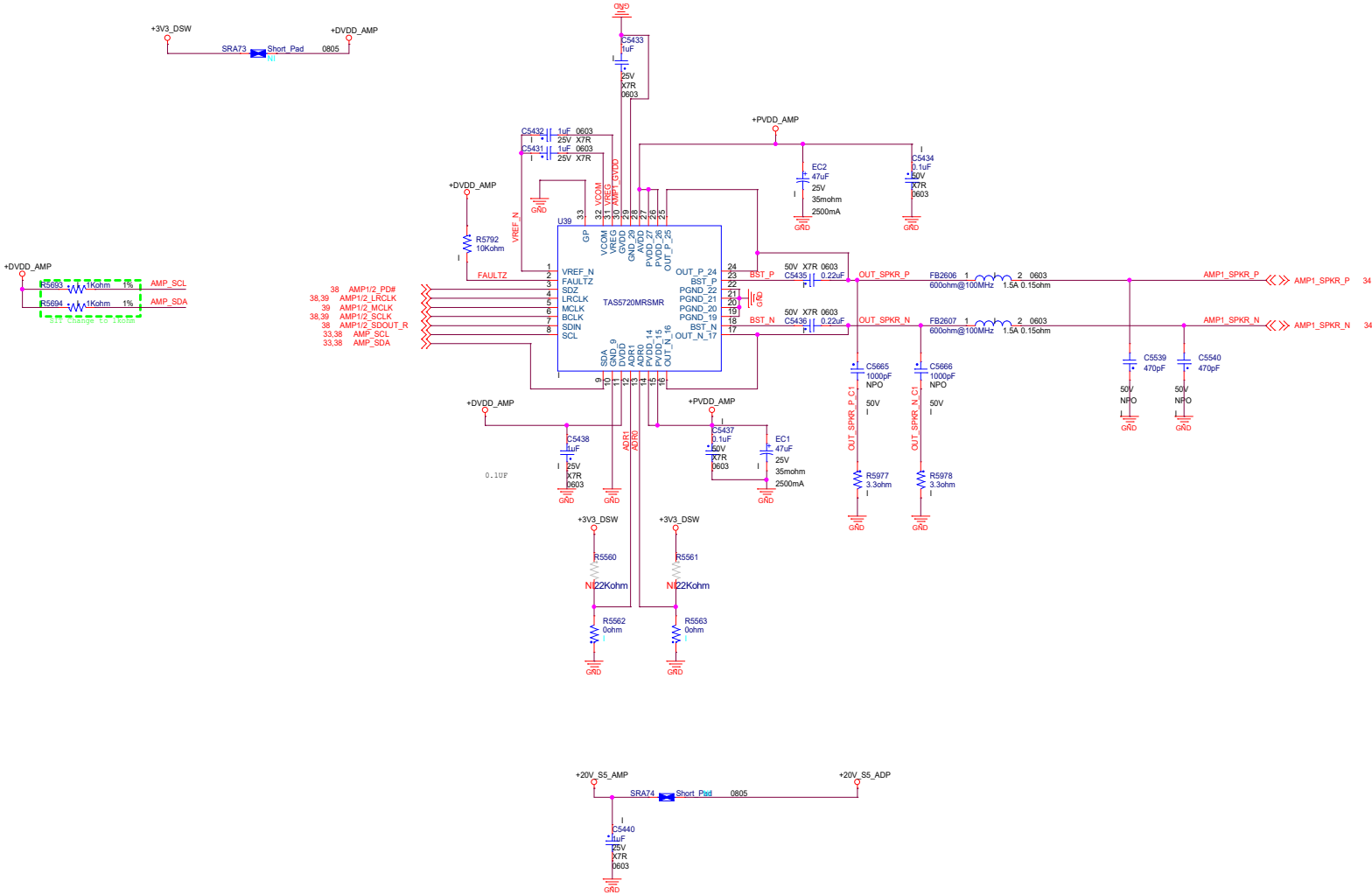
Sheet: 35 of 94



AUDIO COMBO JACK (MIC+HEADPHONE)



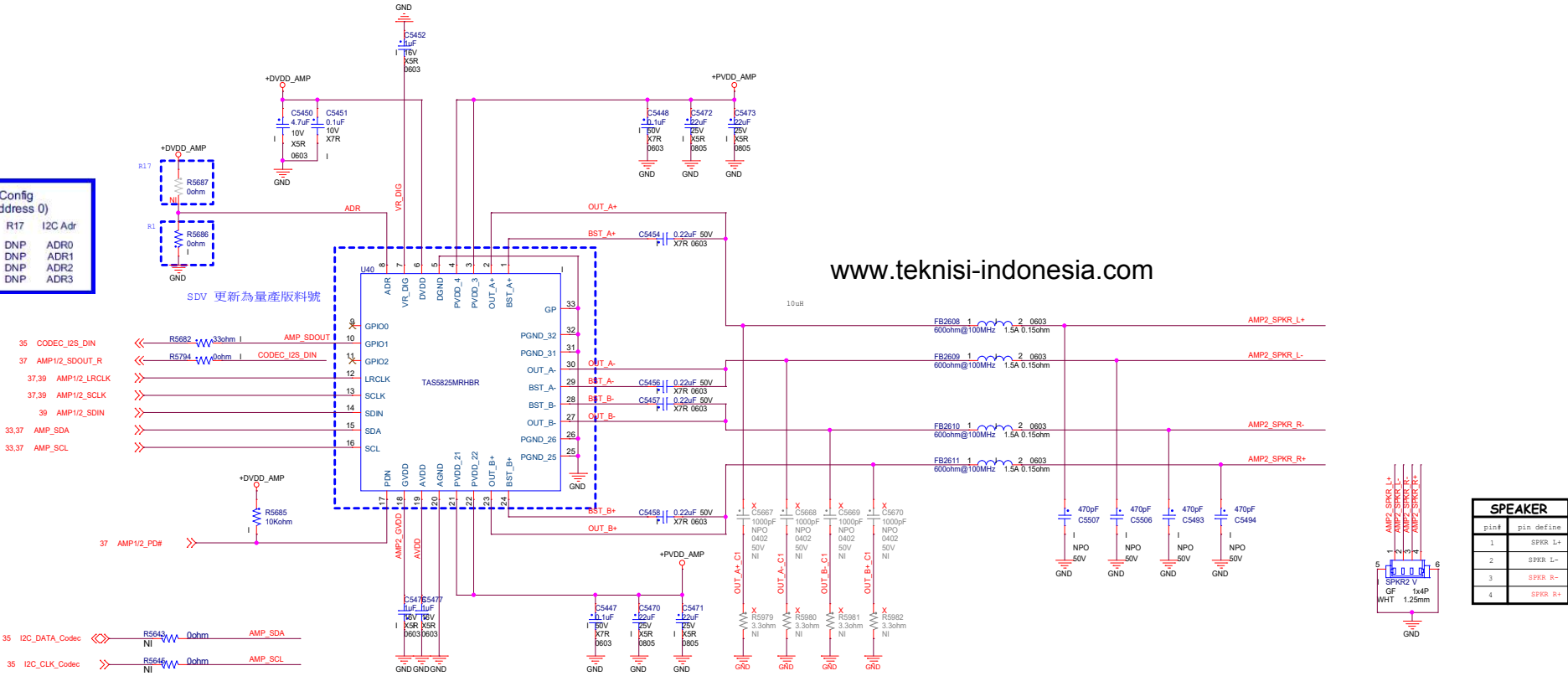
Amp for first set SPKER



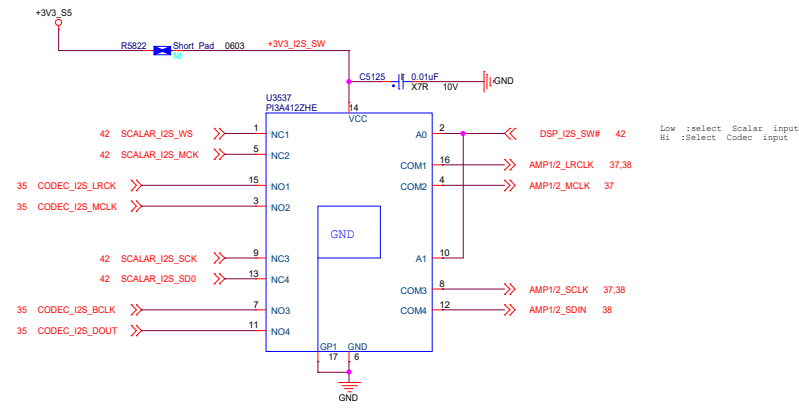
SPEAKER	
pin#	pin define
1	SPKR_P
2	SPKR_N
3	
4	

Amp for 2nd set SPKER

ADR PIN Config (I2C Slave Address 0)			
	R1	R17	I2C Adr
(DEFAULT)	0 ohm	DNP	ADR0
	1k	DNP	ADR1
	4.7k	DNP	ADR2
	15k	DNP	ADR3



CODEC & SCALAR I2S MUX



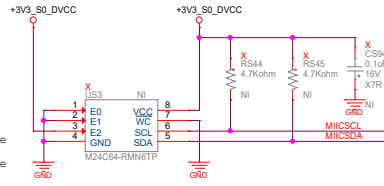
A0	Function	A1	Function
0	NC _X Connected to COM _X	0	NC _Y Connected to COM _Y
1	NO _X Connected to COM _X	1	NO _Y Connected to COM _Y

Notes:
1. X = 1 or 2
2. Y = 3 or 4

eDP TO LVDS - RTD2136

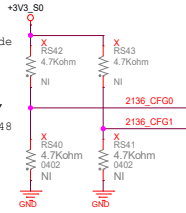
```
EEPROM Mode
In EEPROM mode, an additional
EEPROM is needed.
EEPROM should configure with
following condition.

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte
   addressing device
3- Slave address should configure
   as 0xA8
```

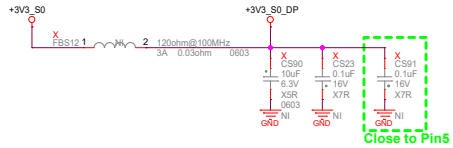
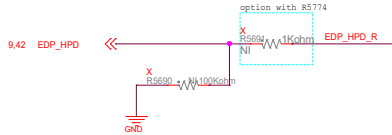


RTD2136 Supports three operation mode
for system design.
Reserved 4.7K resistor pull up/low
for mode selection

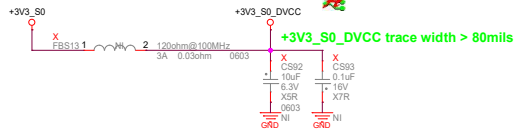
```
ROM ONLY Mode : PIN47 4.7K pull low,
PIN48 4.7K pull high
EP Mode : PIN47 4.7K pull high, PIN48
4.7K pull low
EEPROM Mode : PIN47 4.7K pull high,
PIN48 4.7K pull high
```



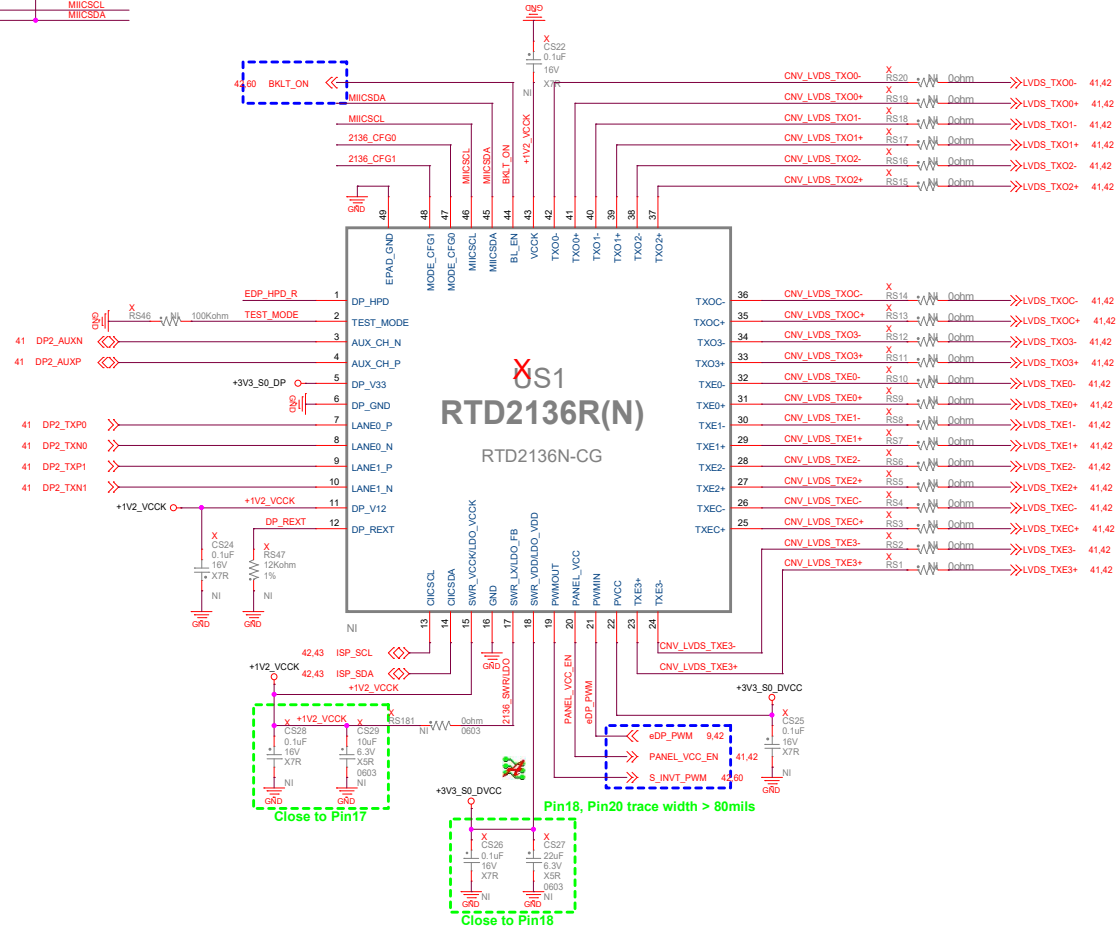
option with R5774



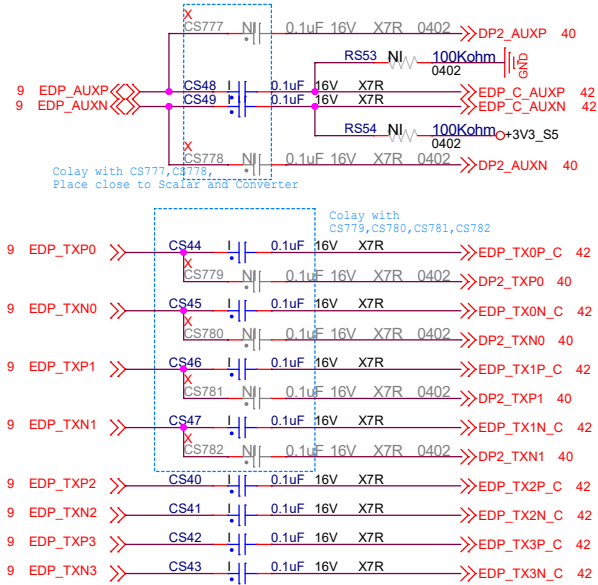
Close to Pin5



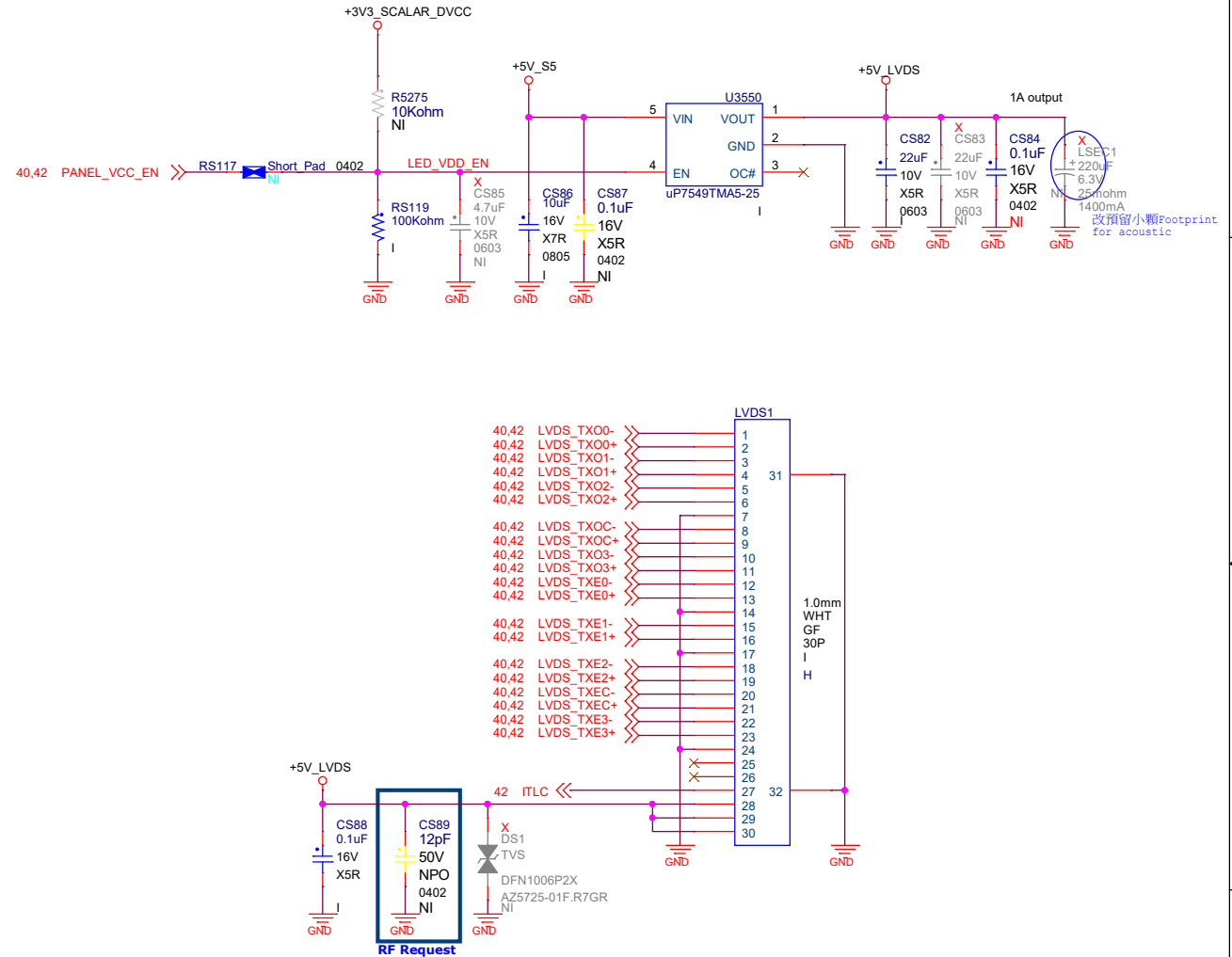
1/3_S0_DVCC trace width > 80mils



SCALAR AND CONVERT SHARE



LVDS CONNECTOR



AVC Asia Vital Components Co.

Title
LVDS Connector

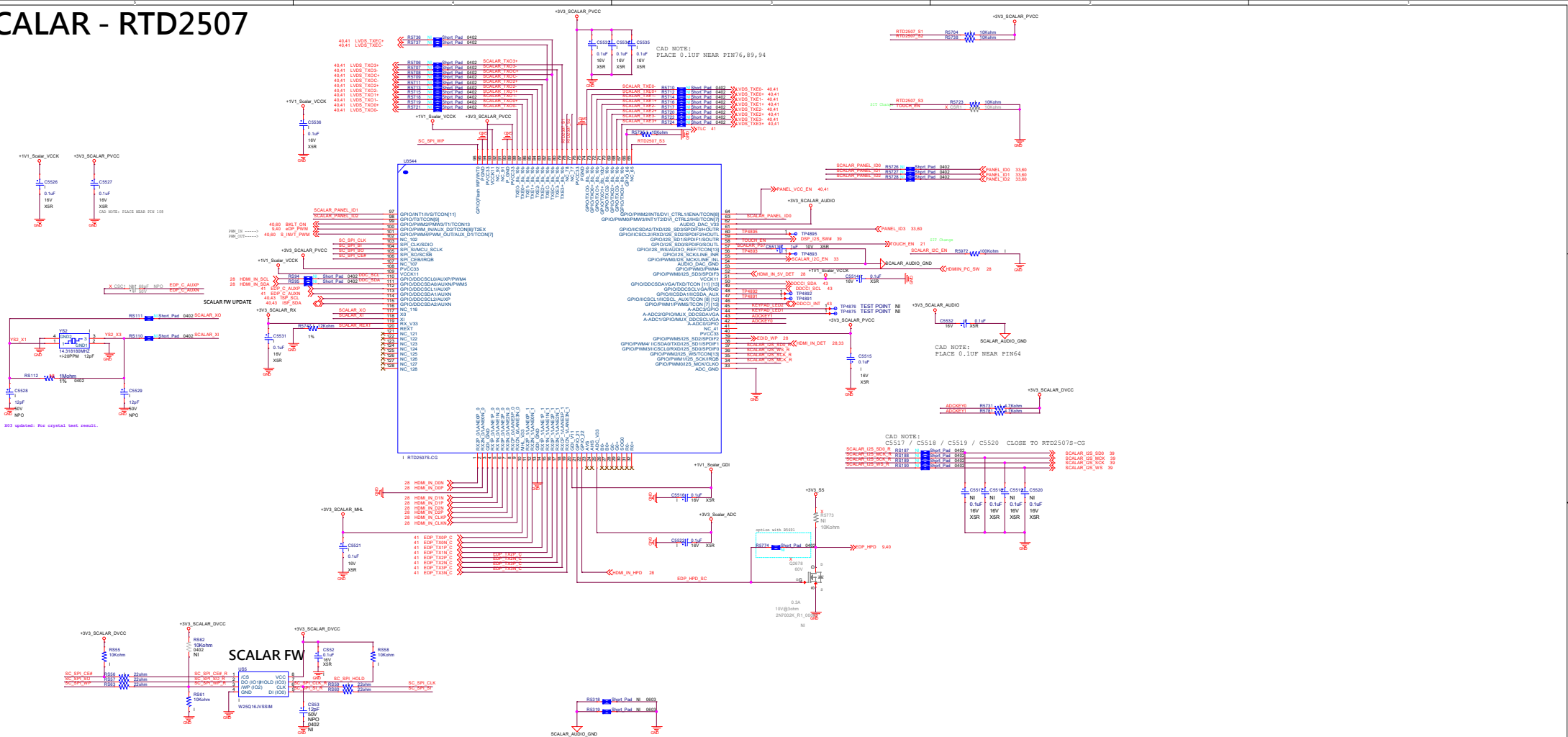
Size B Document Number
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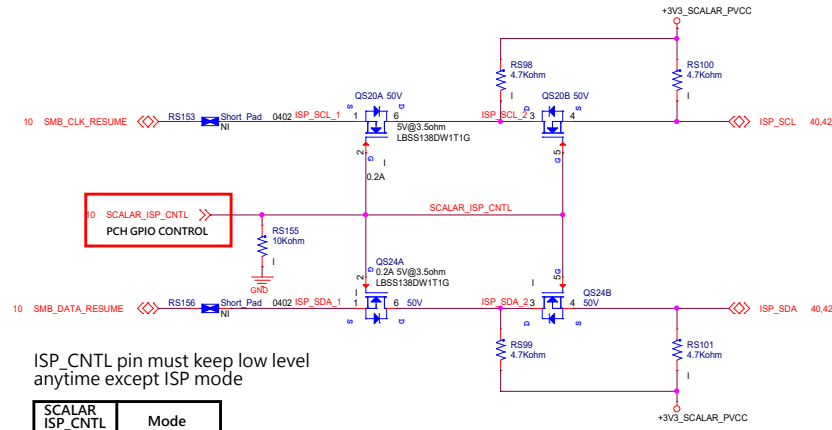
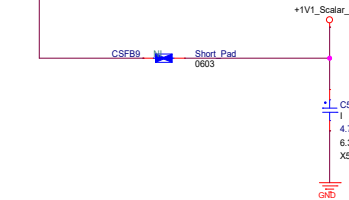
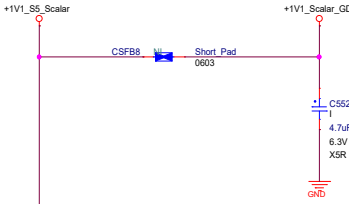
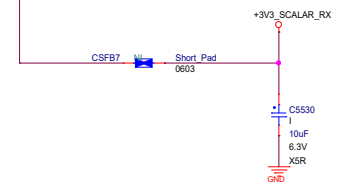
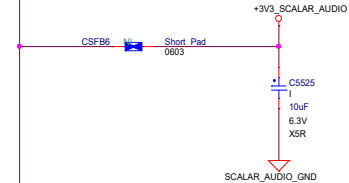
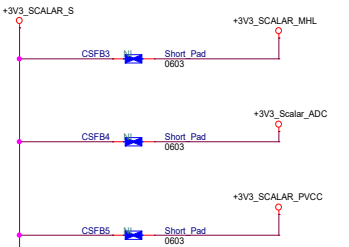
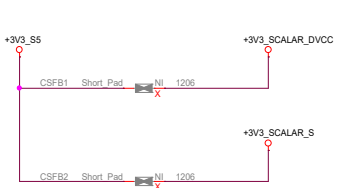
SCALAR - RTD2507



SCALAR POWER

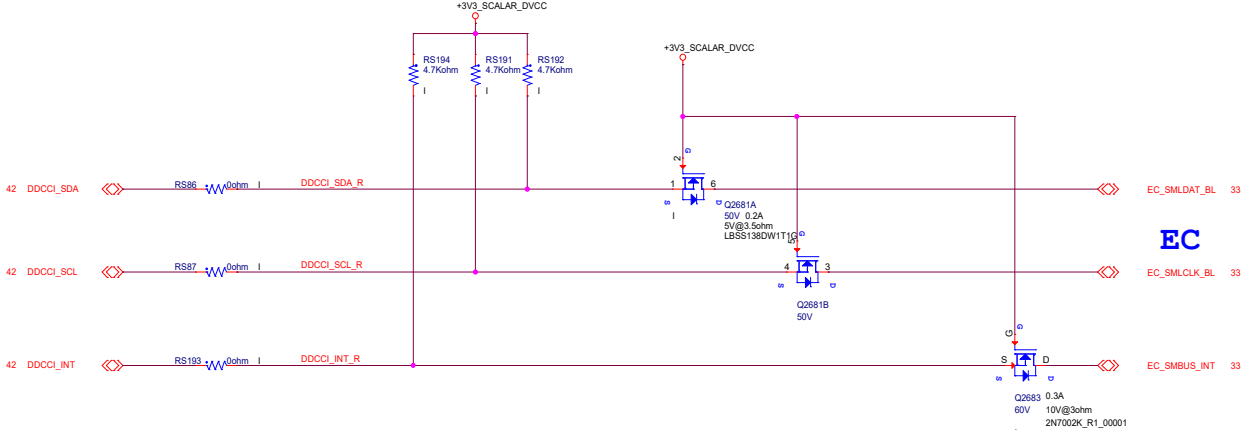
SCALAR FW UPDATE

SCALAR DATA SYNC



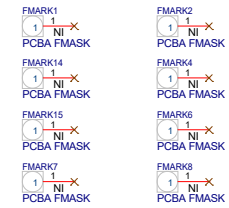
ISP_CNTL pin must keep low level anytime except ISP mode

SCALAR ISP_CNTL	Mode
H	Simultaneous
L	Isolate

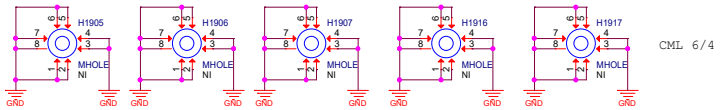


Standoff / Mounting Hole

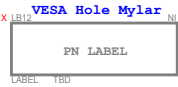
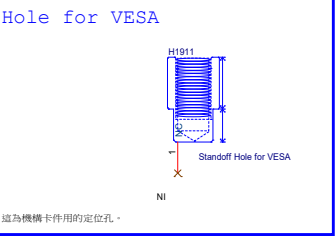
FIDUCIAL MARK



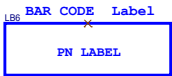
SCREW



FAN SCREW & STAND-OFF



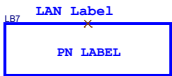
Label



8S Barcode 43x9mm



FRU BARCODE 42x13mm



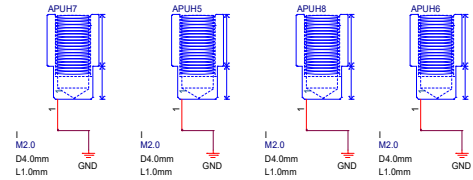
MAC Address 31x5.73mm



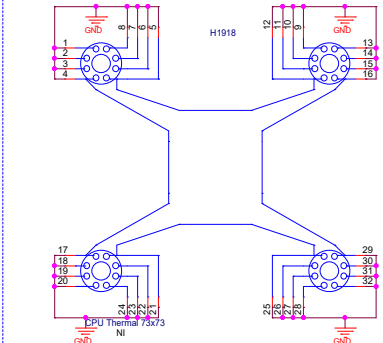
SMT Laser 5x6mm
NI

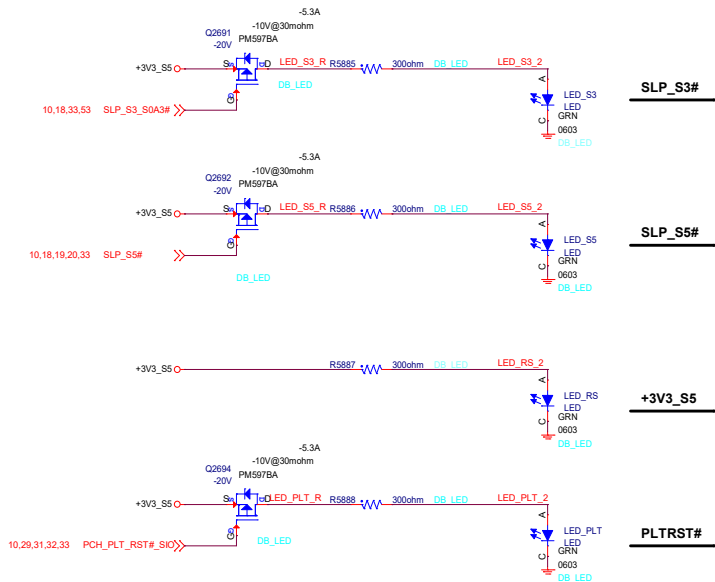


APU Stand off



CPU HEATSINK HOLE





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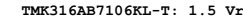
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```

DELAY
10us: Float
50us: GND
100us: VCC (default)

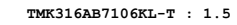
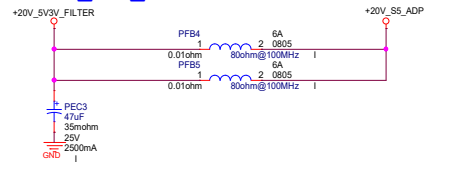
HYS
2mV: Float
4mV: GND
8mV: VCC (default)

LATCH:
OFF: GND (default)
ON: VCC

```



+5V3V_VIN_FILTER



Max Load: 9.1A

Vout	3.3V
Vin	20V
Switch Freq	370KHz
minimum ocp	15.93A
Vin Ripple	10uFx2/1A
Choke size	3.3uH/11.5X10.3mm
Choke Idc/Isat	10A/18.6A
Choke DCR	15mohm
Cin CAP	10uFx2
Cout CAP	220uF,0.1uF
Cout CAP ESR	12mohm
LIR	0.258

TPS51275B OCP Equation :

$$R_{limit} = (I_{limit} - \Delta I_L / 2) * R_{ds(on)} * 8 / I_{cs}$$

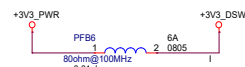
+3V3_S5
Rds(on)= 5.7mohm
Rlimit=60.4k ohm
OCP Ilimit= 14.597A

Vout	5V
Vin	20V
Switch Freq	300KHz
minimum ocp	16.65A
Vin Ripple	10uFx2/1A,47uF/1.4A
Choke size	3.3uH/11.5X10.3mm
Choke Idc/Isat	10A/18.6A
Choke DCR	12mohm
Cin CAP	10uFx2
Cout CAP	220uF,0.1uF
Cout CAP ESR	15mohm
LIR	0.379

TPS51275B OCP Equation :

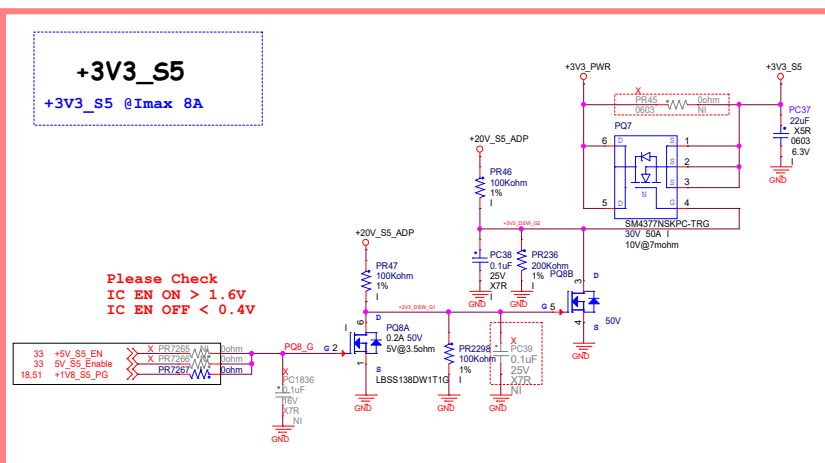
$$R_{limit} = (I_{limit} - \Delta I_L / 2) * R_{ds(on)} * 8 / I_{cs}$$

+5V_S5
Rds(on)= 5.7mohm
Rlimit=66.5k ohm
OCP Ilimit= 16.65A



+3V3_S5

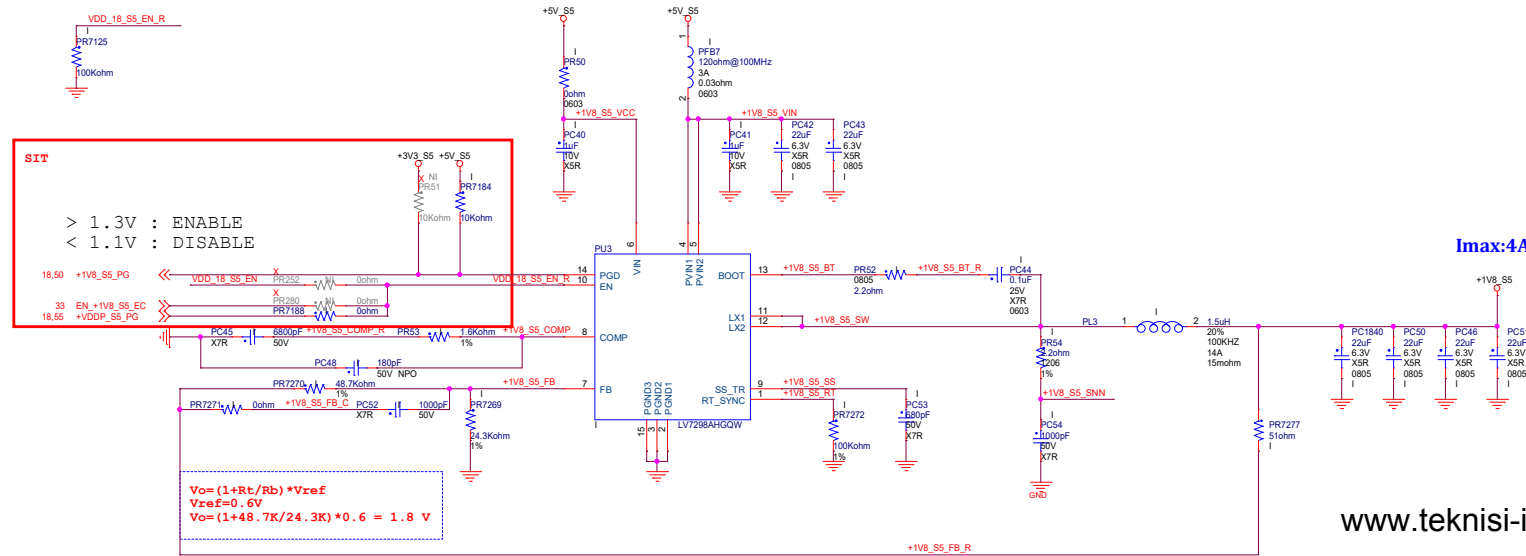
+3V3_S5 @Imax 8A



Please Check
IC EN ON > 1.6V
IC EN OFF < 0.4V

33	+5V_S5_EN	X	PR7265	
33	5V_S5_Enable	X	PR7266	
18,51	+1V8_S5_PG		PR7267	

+1V8_S5



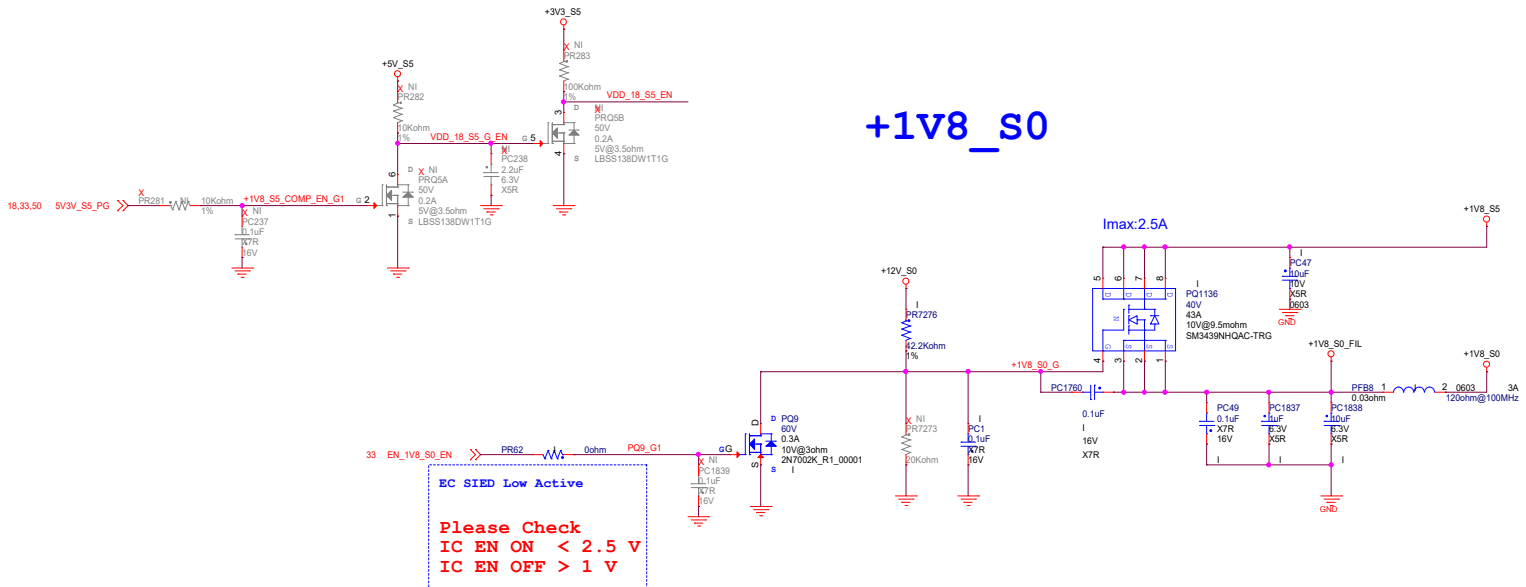
Max Load: 4A CONVERTER

Vout	1.8V
Vin	5V
Switch Freq	500KHz
ocp	8A
Vin_ripple	22uF/2A x 2
Choke size	2.2uH/7.6x6.8mm
Choke Idc/Isat	9A/14A
Choke DCR	20mohm
Cin CAP	22uFx2
Cout CAP	22uFx4
Cout CAP_ESR	
LIR	

I_{max}:4A

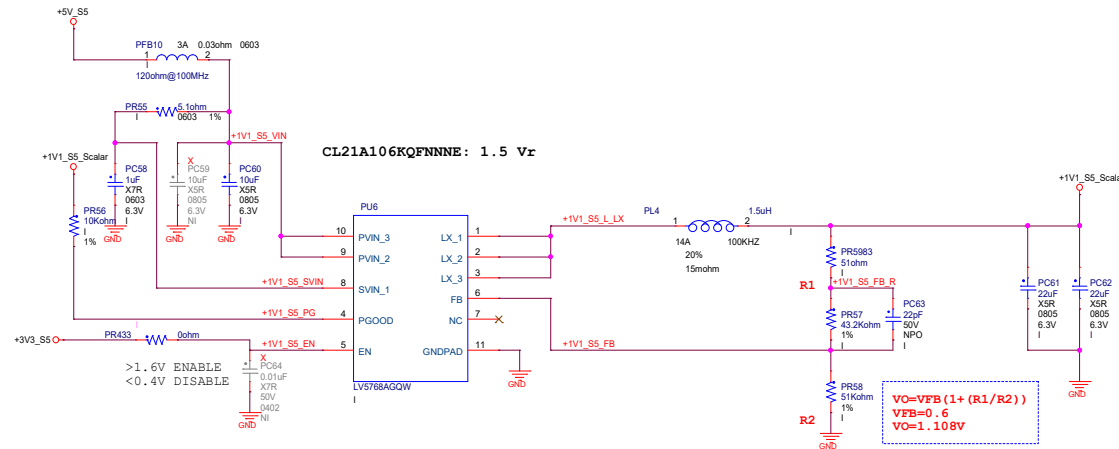
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+1V8_S0



I_{max}:2.5A

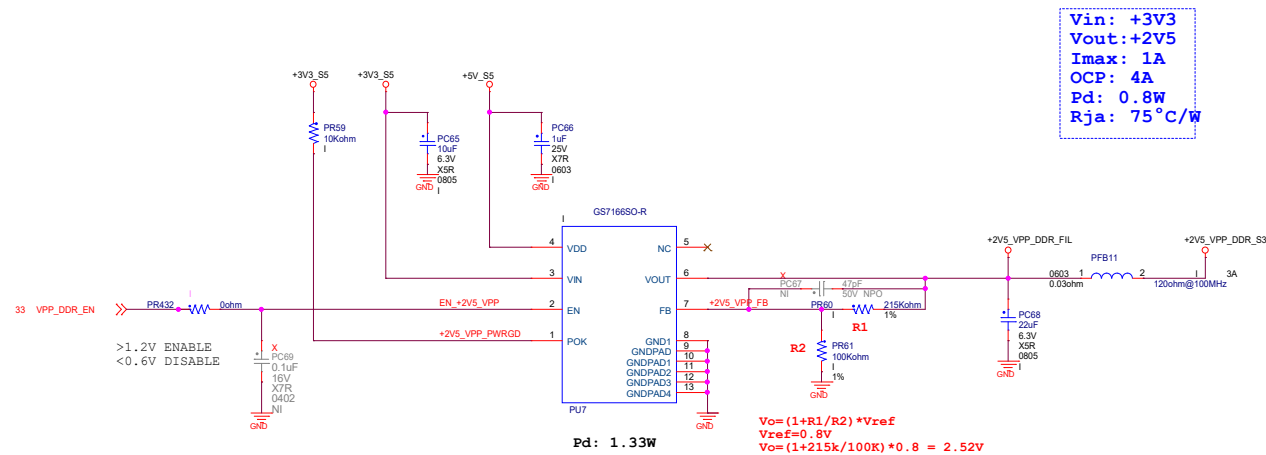
+1V1_S5_Scalar



Max Load: 0.5A CONVERTER

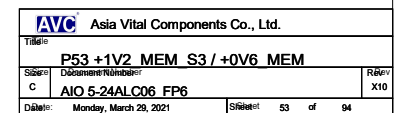
Vout	1.1V
Vin	5V
Switch Freq	1MHz
ocp	6.5A
Vin_Iripple	10uF/1A
Choke size	1.5uH/7.6x6.8mm
Choke Idc/Isat	9A/14A
Choke DCR	15mohm
Cin CAP	10uF
Cout CAP	22uF x2
Cout CAP ESR	
LIR	

+2V5_VPP_DDR



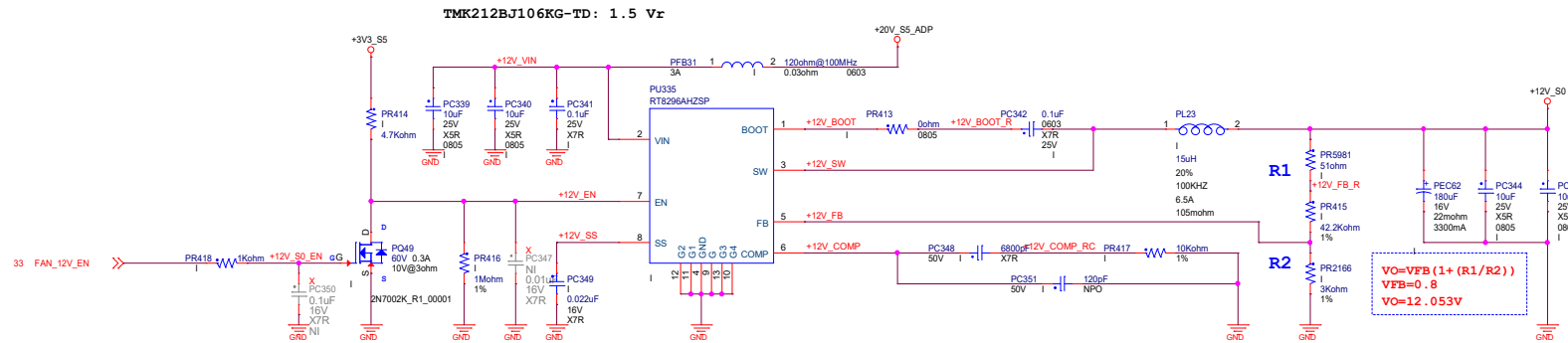
+1V2_DDR4_S3

Vout	1.2V
Vin	20V
Switch Freq	400KHz
oep	15.3A
Vin Ripple	10uFx2/1A
Choke size	1.5uH/7.3X6.8mm
Choke Idc/Isat	9A/14A
Choke DCR	15mohm
Cin CAP	10uFx2
Cout CAP	390uF,22uF
Cout CAP ESR	10mohm
LIR	

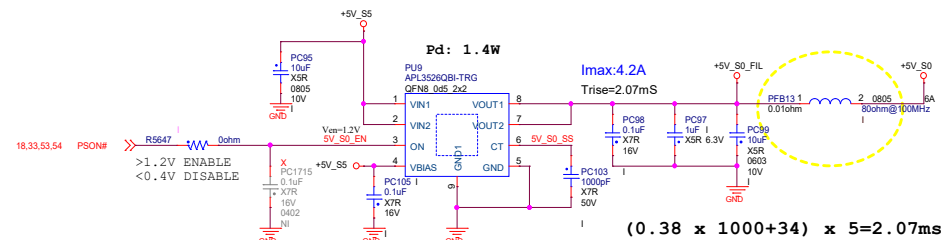


+12V_S0

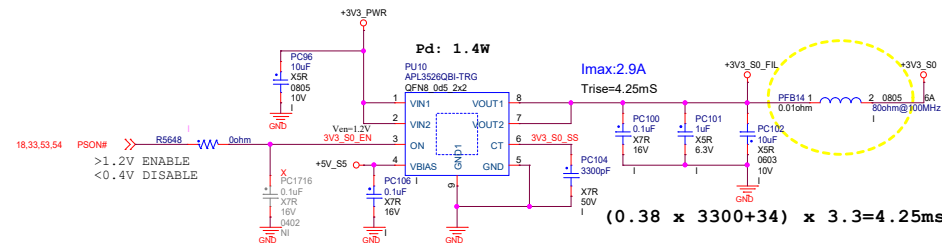
Max Load:1.2A



+5V_S0



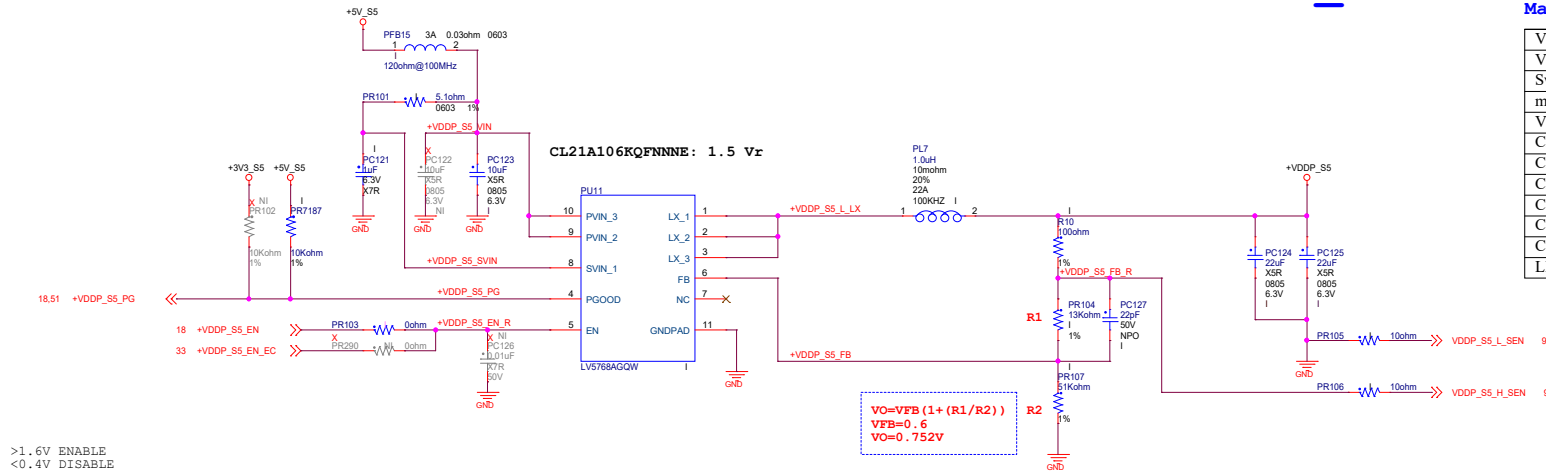
+3V3_S0



+VDDP_S5

Max Load: 2A

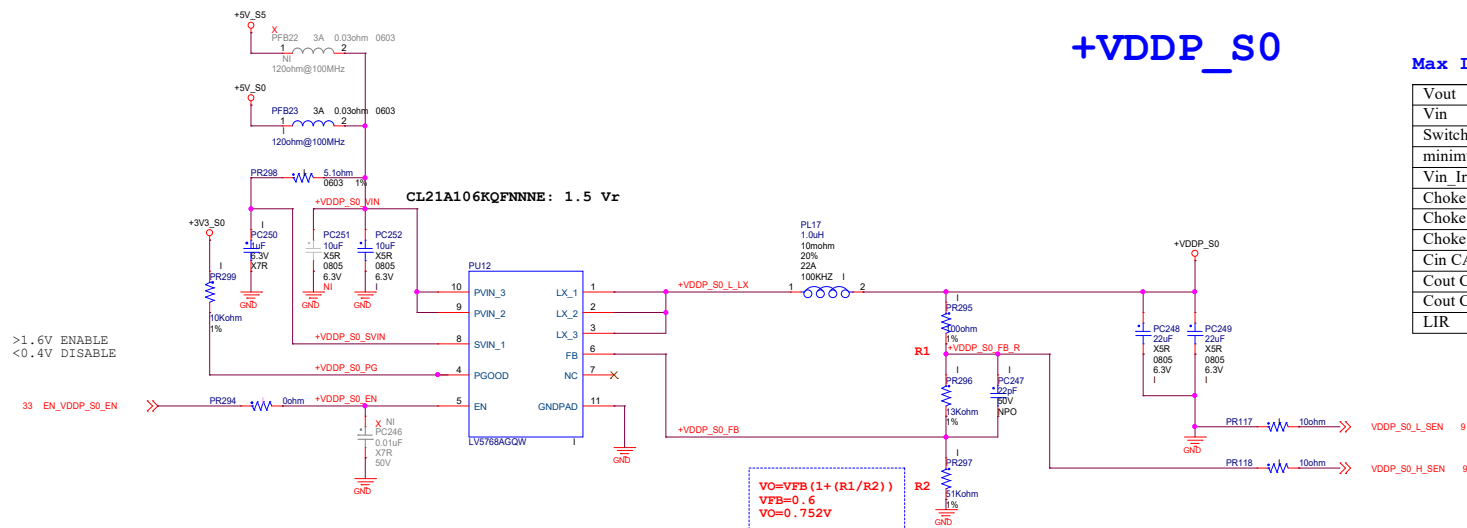
Vout	0.75V
Vin	5V
Switch Freq	1MHz
minimum ocp	8A
Vin Ripple	10uFx2/1A
Choke size	1uH/7.6X6.8mm
Choke Idc/Isat	11A/22A
Choke DCR	10mohm
Cin CAP	10uFx1
Cout CAP	22uFx2
Cout CAP_ESR	
LIR	0.319



+VDDP_S0

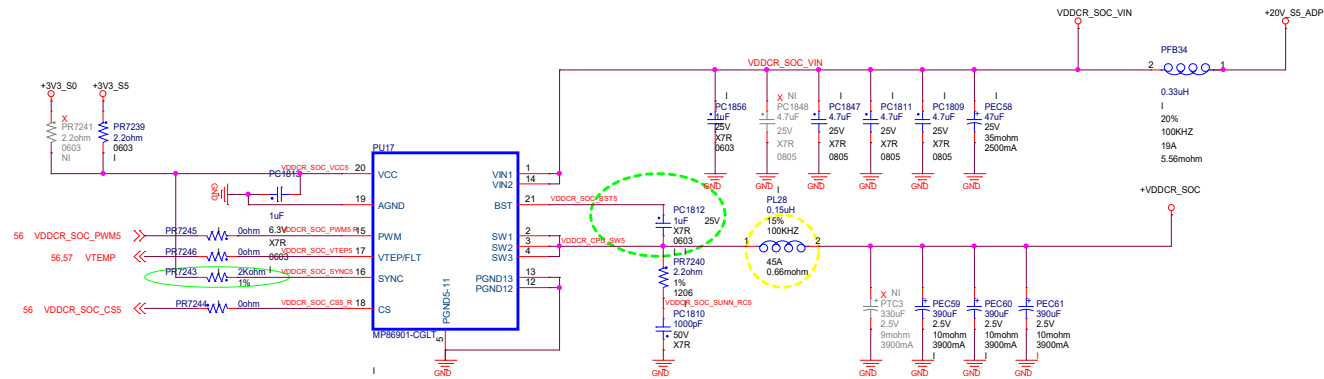
Max Load: 2A

Vout	0.75V
Vin	5V
Switch Freq	1MHz
minimum ocp	8A
Vin Ripple	10uFx2/1A
Choke size	1uH/7.6X6.8mm
Choke Idc/Isat	11A/22A
Choke DCR	10mohm
Cin CAP	10uFx1
Cout CAP	22uFx2
Cout CAP_ESR	
LIR	0.319



+VDDCR_SOC

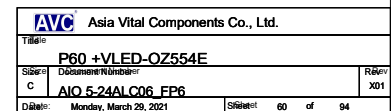
Vin: +20V_S5_ADP
Vout: +VDDCR_SOC
DC Loadline: 2.1mohm
TDC: 13A
Imax: 17A
OCP: 40A



Vout	0.9V
Vin	20V
Switch Freq	400KHz
minimum ocp	40A
Vin_Ripple	10uFx2/1A, 47uFx1/2.5A
Choke size	0.15uH/7.6x6.8mm
Choke Idc/Isat	36A/45A
Choke DCR	0.66mohm
Cin CAP	10uFx2 + 47uFx1
Cout CAP	390uFx3 + 330uFx1
Cout CAP_ESR	10mohmx3 // 9mohmx1
LIR	

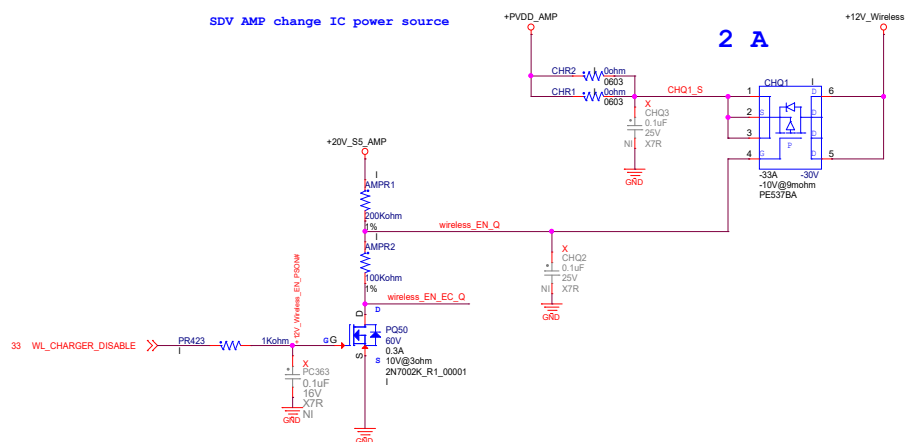
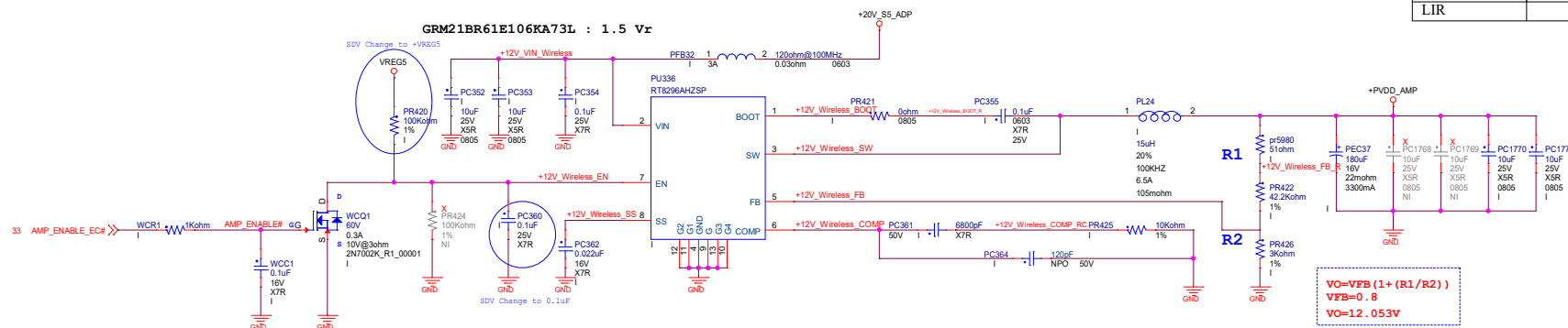
Max Load:0.26A

Vout	Depend on panel
Vin	20V
Switch Freq	400KHz
ocp	3.3A
Vin_Iripple	10uFx4/1A
Choke size	15uH/7.6X7.1mm
Choke Idc/Isat	6.8A/7.5A
Choke DCR	50mohm
Cin CAP	10uFx4
Cout CAP	22uF,2.2uF
Cout CAP_ESR	
LIR	



Max Load: 2A

Vout	12V
Vin	20V
Switch Freq	340KHz
ocp	5.1A
Vin_ripple	10uFx2/1A
Choke size	15uH/7.6x6.8mm
Choke Idc/Isat	3A/6.5A
Choke DCR	105mohm
Cin CAP	10uFx2, 0.1uF
Cout CAP	180uFx1, 10uFx2
Cout CAP ESR	
LIR	



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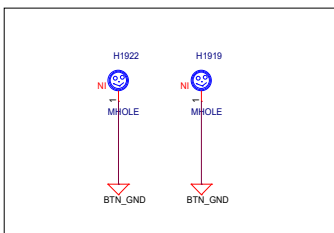
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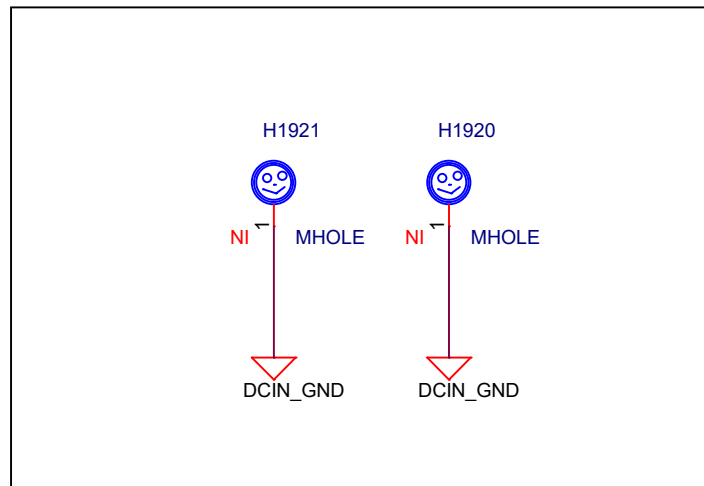
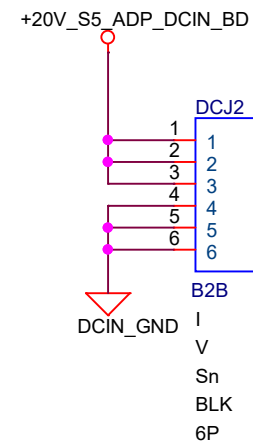
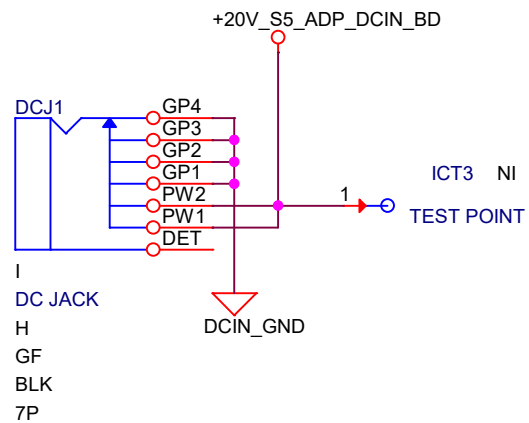
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0304Y22 P 009 CHM1C,CHM2C,CHM2C,CHM1C,CHM1C,CHM2C,CHM1C Change to NI to Remove SD Cards Function
0304Y21 P 045 LED_S3,LED_S5,LED_S2,LED_FLT,Q0691,Q0692,Q0694,SM1 Change to NI to Remove Debug LED
0329Y21 P 001 FI Change to NI, T001,T002,T001 Change to I for BOE Touch panel selection
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	S0/S1	S3	S4/S5
LED STATE	ON	BLINKING	OFF



FMARK13

1

NI

PCBA FMASK

FMARK10

1

NI

PCBA FMASK



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Title

DC IN

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